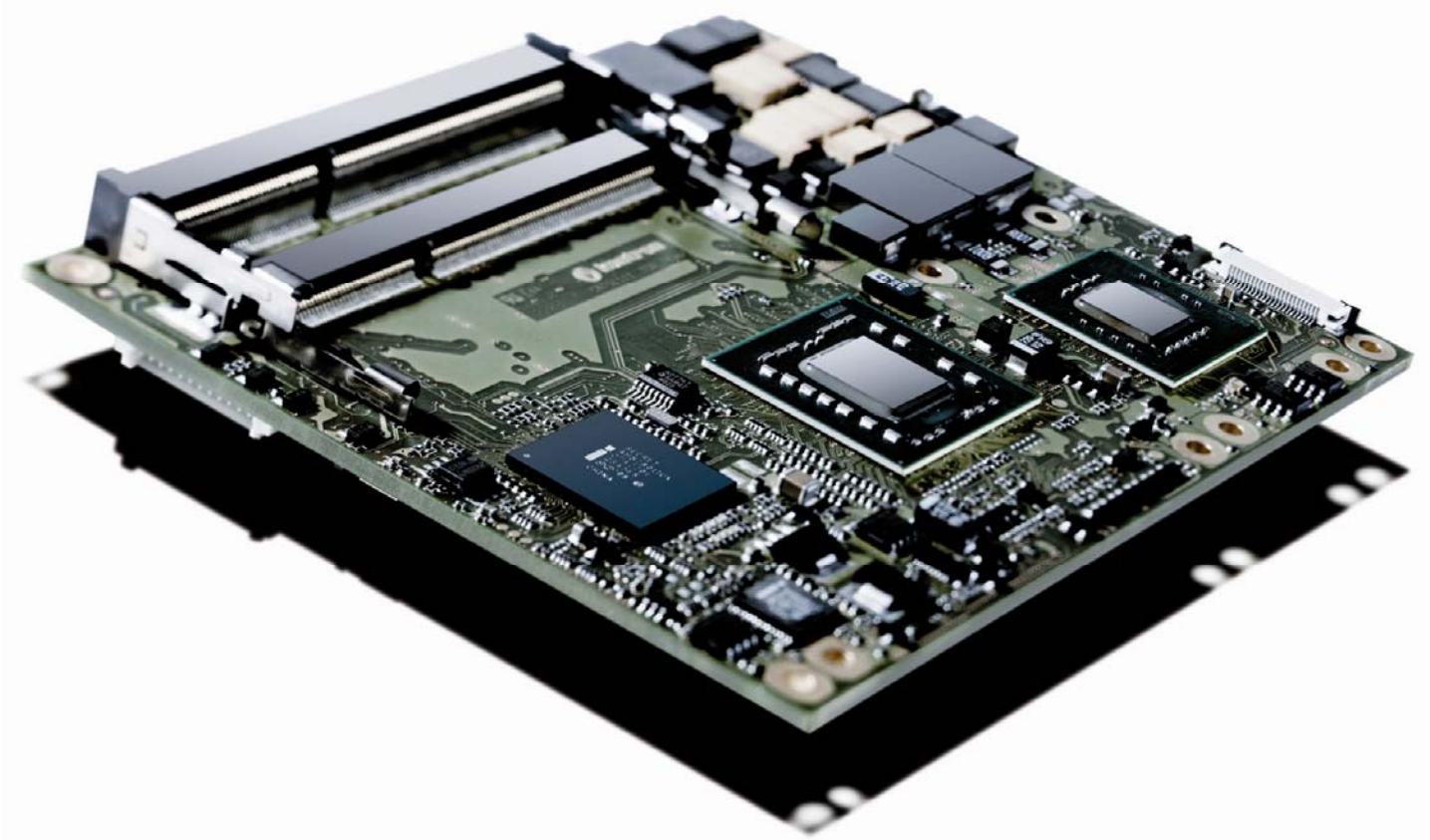
Kontron User's Guide



ETXexpress®-PC

Document Revision 1.0
All not approved entries are marked!

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1 User Information

1.1 About This Document

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- Microsoft is a registered trademark of Microsoft Corp.
- Intel is a registered trademark of Intel Corp.
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1.4 Standards

Kontron Embedded Modules GmbH is certified to ISO 9000 standards.

1.5 Warranty

This Kontron Embedded Modules GmbH product is warranted against defects in material and workmanship for the warranty period from the date of shipment. During the warranty period, Kontron Embedded Modules GmbH will at its discretion decide to repair or replace defective products.

Within the warranty period, the repair of products is free of charge as long as warranty conditions are observed.

The warranty does not apply to defects resulting from improper or inadequate maintenance or handling by the buyer, unauthorized modification or misuse, operation outside of the product's environmental specifications or improper installation or maintenance.

Kontron Embedded Modules GmbH will not be responsible for any defects or damages to other products not supplied by Kontron Embedded Modules GmbH that are caused by a faulty Kontron Embedded Modules GmbH product.

1.6 Technical Support

Technicians and engineers from Kontron Embedded Modules GmbH and/or its subsidiaries are available for technical support. We are committed to making our product easy to use and will help you use our products in your systems.

Please consult our Web site at http://www.kontron.com/support for the latest product documentation, utilities, drivers and support contacts. In any case you can always contact your board supplier for technical support.

2 Introduction

2.1 ETXexpress®-PC

Based on the COM Express standard, Kontron's ETXexpress®-PC, powered by a variety of Intel®'s Core2Duo® and CeleronM® processors, is a next-generation embedded module that brings advanced technology to tomorrow's applications, as well as continuing today's legacy devices. Built around serial differential signaling technologies, ETXexpress®-PC modules incorporate the following interfaces into 95 x 125 small form factor embedded module:

- PCI Express, which provides a high performance I/O infrastructure with transfer rates starting at 2.5 Giga transfers per second over a x1 PCI Express lane
- PCI
- Serial ATA (SATA II)
- USB 2.0
- LVDS
- Azalia High Definition Audio
- Advanced Configuration and Power Interface (ACPI) for optimized power management

The ETXexpress®-PC is built around the Intel® Core2Duo® and CeleronM® processor and the Intel® GS45 chipset. These modules feature the most current desktop features such as USB 2.0, SATA, and PCI Express buses.
The ETXexpress®-PC delivers up to 8GB DDR3 RAM. For applications that require advanced real-time video capabilities, the ETXexpress®-PC has integrated graphics with 2D, 3D and Motion Video Acceleration and also supports PCI Express graphics, two SDVO ports or two HDMI capable DVI ports. Fast communications are possible courtesy of a Gigabit Ethernet port.
The ETXexpress®-PC supports up to 6 PCI Express x1 Lanes and PCI Express cards (only when 10/100MB Ethernet is equipped) as well as established hardware solutions based on current buses such as 32-bit PCI. A Gigabit Ethernet port provides fast connectivity to LAN/WAN and 8 USB 2.0 ports provide fast and sufficient interfaces for external peripherals.
ETXexpress®-PC modules also provide the following interfaces that are always located in the same physical position on each board:
PCI-express, PCI32, USB, serial ATA (SATA), parallel ATA (PATA), LVDS Multi Media ports, as well as an ACPI (Advanced Configuration and Power Interface) for optimized power management. Mounting holes on the board provide secure mounting to allow the module increased shock and vibration resistance.

2.2 ETXexpress®-PC Module Overview

The international COM Express standard defines two new form factor sizes: Basic and Extended. The primary difference between the Basic and Extended size is a larger board size and thermal envelope in the Extended size. The ETXexpress®-PC follows the basic form factor.

Five module Pin-out Type definitions exist for Basic and Extended modules. Pin-out Types 1-5 apply to Basic and Extended module form factors. Pin-out Types 1-5 offer different functionalities. For a complete explanation of the features of each of the Pin-out Types 1-5, please see the COMexpress Specification.

The ETXexpress®-PC uses the Pin-out Type 2 architecture, which includes PCI and IDE interfaces. These modules either use onboard graphics capabilities or may use 8 PEG lanes to connect to an external video controller. In case of onboard graphics, PEG pins may be alternatively used for SDVO or DVI ports.

Pin-out Type 2 features include:

- Dual 220 pin connectors (Primary Connector: Rows A-B and Secondary Connector: Rows C-D, 440 pins total)
- 32-bit PCI interface
- IDE port (to support legacy ATA devices)
- Up to 6 PCI Express general purpose lanes
- One, x16 PCI Express Graphics (PEG) slot
- Up to 8 USB 2.0 ports; 4 shared over-current lines
- Up to 4 Serial ATA ports
- Dual 18-bit LVDS channels (with 24 bit dithering)
- Analog VGA and TV Out: Composite Video, S-Video, Component Video (YPbPr)
- High Definition Audio digital audio interface (external CODEC)
- Single Gigabit Ethernet interface with integrated PHY
- +12V primary power supply input, +5V standby and 3 V RTC power supplies

2.3 Understanding ETXexpress® functionality

All Kontron ETXexpress® modules contain two connectors; each of it has two rows. The primary connector has two rows called Row A and Row B. The secondary connector has two rows called Row C and Row D.

The primary connector (Row A and Row B) feature the following legacy-free functionality:

- Ethernet
- Serial ATA (SATA)
- USB 2.0
- LVDS/VGA and dual display video
- Intel High Definition Audio (Azalia)
- LPC (low pin count) Bus

The secondary connector (Row C and Row D) provides support for the following buses and I/O:

- PCI Express
- PCI
- IDE

2.4 ETXexpress® Documentation

This product manual serves as one of three principal references for an ETXexpress® design. It documents the specifications and features of ETXexpress®-PC. The other two references, which are available from your Kontron Support or from PICMG®, include:

- The COMexpress Specification defines the ETXexpress® module form factor, pinout, and signals.
- The ETXexpress® Component SBC™ Design Guide serves as a general guide for baseboard design, with a focus on maximum flexibility to accommodate a wide range of ETXexpress® modules.

Note: Some of the information contained within this product manual applies only to certain product revisions (CE: xxx). If certain information applies to specific product revisions (CE: xxx) it will be stated. Please check the product revision of your module to see if this information is applicable.

2.5 ETXexpress® Benefits

Embedded technology extended express (ETXexpress) modules are very compact (125 x 95 mm, 12mm thick), highly integrated computers. All ETXexpress® modules feature a standardized form factor and a standardized connector layout that carry a specified set of signals. Each ETXexpress® module is based on connector type 2 of the COMexpress specification. This standardization allows designers to create a single-system baseboard that can accept present and future ETXexpress® modules.

ETXexpress® modules include common personal computer (PC) peripheral functions such as:

- Graphics
- USB ports
- Ethernet
- Sound
- IDE (and SATA)

The baseboard designer can optimize exactly how each of these functions implements physically. Designers can place connectors precisely where needed for the application on a baseboard designed to optimally fit a system's packaging.

A peripheral PCI bus can be implemented directly on the baseboard rather than on mechanically unwieldy expansion cards. The ability to build a system on a single baseboard using the computer as one plug-in component simplifies packaging, eliminates cabling, and significantly reduces system-level cost.

A single baseboard design can use a range of ETXexpress® modules. This flexibility can differentiate products at various price/performance points, or to design future proof systems that have a built-in upgrade path. The modularity of an ETXexpress® solution also ensures against obsolescence as computer technology evolves. A properly designed ETXexpress® baseboard can work with several successive generations of ETXexpress® modules.

An ETXexpress® baseboard design has many advantages of a custom, computer-board design but delivers better obsolescence protection, greatly reduced engineering effort, and faster time to market.

3 Specification

3.1 Functional Specification

Processor

- Intel® Core2Duo Processor (Penryn)

Bus

- Up to 1066 MHz CPU bus (depends on used processor)
- Up to 1066 MHz memory bus (depends on used processor and memory)

Processor features

- Support for SSE, SSE2, SSE3, SSE4.1, MMX™
- Supports Intel® architecture with Intel® Wide Dynamics Execution
- Supports L1 chache-to-cache (C2C) transfer
- Advanced power management features including Enhanced Intel SpeedStep® Technology and dynamic FSB frequency switching
- Intel® 64 architecutre
- Supports enhanced Intel Virtualization Technology
- Enhanced Intel® Dynamic Acceleration
- Intel® Deep Power Down low-power state with P_LVL6 I/O Support
- Support for Intel® Trusted Execution Technology

Processor cache l2

- 6 MB or 3 MB on-die 2nd level cache (depends on used processor)

Chipset

- Intel® GS45
- Intel® ICH-9M

Memory

- Dual channel DDR3-SO-DIMM which allows up to 8GB RAM

PCI Express Graphics (PEG): Intel® GS45

- One 16-lane PCI Express port for external PCI Express based graphic cards

PCI Express: Intel® ICH-9M

- 5 PCI Express x1 lanes

PCI32: Intel® ICH-9M

- Parallel PCI Bus 32 bit MHz according to PCI2.3

IDE: Intel® ICH-9M

- Single PATA channel support

- Supports PIO, Multi-Word DMA and Ultra-DMA 33/66/100/133 modes

Serial ATA: Intel® ICH-9M

- 4 Channels Serial ATA
- SATA Spec. Rev. 2.0 up to 300MB/s per channel
- SATA II (AHCI)

Feature	AHCI disabled	AHCI enabled
Native Command Queuing (NCQ)	N/A	Supported
Auto Activate for DMA	N/A	Supported
Hot Plug Support	N/A	Supported
Asynchronous Signal Transfer	N/A	Supported
3 Gb/s Transfer Rate	Supported	Supported
ATAPI Asynchronous Notification	N/A	Supported
Host & Link Initiated Power Management	N/A	Supported
Staggered Spin-Up	Supported	Supported
Command Completion Coalescing	N/A	N/A
Port Multiplier	N/A	Supported
External SATA	N/A	Supported

Universal Serial Bus: Intel® ICH-9M

- 8 USB 1.1/2.0 ports (UHCI and EHCI)
- USB legacy keyboard support
- USB floppy, CD-ROM, Hard drive and memory stick boot support

Gigabit Ethernet: Intel® 82567

- Fully compatible with IEEE 802.3, IEEE 802.3u, IEEE 802.3ab

Internal Graphics: Intel® 82567

- Onboard video graphics array: Intel® GS45
- Intel Gen 5.0 integrated graphics engine with 10 fully programmable cores
- 533-MHz core render clock @ 1.05-V core voltage
- Supports iHDMI/DVI, DP, TV-Out, LVDS, CRT and SDVO
- Intel® Dynamic Video Memory Technology (Intel® DVMT 5.0)
- Video Capture via x1 concurrent PCI Express port
- PAVP (Protected Audio-Video Path) support for Protected Intel® HD Audio (Video
- and Audio) Playback
- High performance MPEG-2 decoding
- WMV9 (VC-1) and H.264 (AVC) support
- Hardware acceleration for MPEG2 VLD/iDCT
- Microsoft DirectX*10 support
- Blu-ray* support @ 40 Mb/s

- Hardware motion compensation
- Intermediate Z in classic rendering

Dual-Channel LVDS: Intel® 82567

- 25-112-MHz single/dual-channel
  - Single channel LVDS interface support: 1 x 18 bpp OR 1 x 24 bpp (Type 1 only, compatible with VESA LVDS color mapping)
  - Dual-channel LVDS interface support:2 x 18 bpp OR 2 x 24 bpp panel support
  - TFT panel type supported
- Pixel dithering for 18-bit TFT panel to emulate 24-bpp true color displays
- Panel Fitting. Panning and Center mode supported
- Standard Panel Working Group (SPWG) v.3.5 specification compliant
- Spread spectrum clocking support
- Panel power sequencing support
- Integrated PWM interface for LCD backlight inverter control

DisplayPort (DP) : Intel® 82567

The GMCH supports three DP ports muxed on the PCI Express interface

- 1.62 Gb/s and 2.7 Gb/s
- 1, 2 or 4 data lanes
- 8b 10b coding
- Hot-Plug detect support
- HDCP support

Integrated HDMI (iHDMI) : Intel® 82567

- DVI also supported on same interface
- Single TMDS Link
- 8 bpc only supporting RGB - no YCrCb4:4:4 and YCrCb4:2:2 support
- Data Island Packets including null, AVI Infoframe, audio samples and more
- Video support for CEA modes 480i/p, 576i/p, 720p, 1080i/p and PC modes though dot clock
- HDMI Source only – not a receiver device
- HDCP support
- Support for HDMI repeaters
- Intel HD Audio support
  - Integrated Intel HD Audio codec
  - Dolby* AC3 compress, Dolby* Digital, Dolby* DTS (full support)
  - PCM audio support

SDVO Ports: Intel® 82567

- Two SDVO ports supported
  - SDVO pins are muxed onto the PCI Express Graphics-attach port pins
  - DVI 1.0 support for External Digital Monitor
  - Downstream HDCP Support but no upstream HDCP support
  - Display Hot-Plug support
- Supports appropriate external SDVO components (HDMI, DVI, LVDS, TV-Out)
- I2C channel provided for control

Analog CRT: Intel® 82567

- Integrated 300-MHz DAC
- Analog monitor support up to QXGA
- Support for CRT Hot-Plug

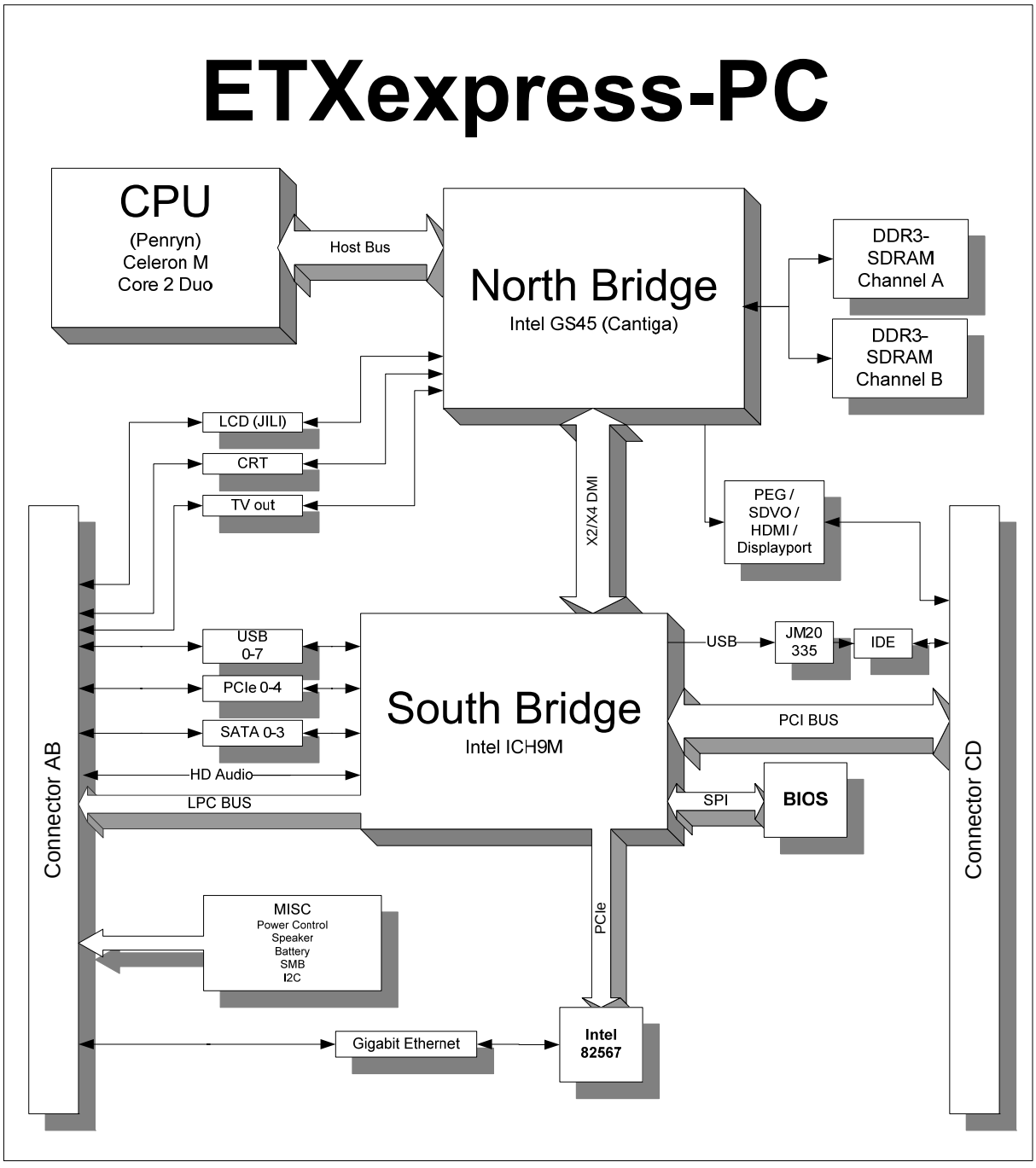
TV-Out: Intel® 82567

- MacroVision not supported
- Overscaling
- NTSC/PAL
- Component, S-Video and Composite Output Interfaces
- HDTV graphics mode support

HD Audio: Intel® ICH-9M

- Up to 3 bit sample depth
- Up to 192 kHz sample rate
- Supports up to 4 codecs

3.1.1 Block Diagram



3.2 Mechanical Specification

Dimension

- 95.0 x 125.0 mm
- Height approx. 12 mm (0.4")

3.3 Electrical Specification

Supply Voltage

- 12 DC +/- 5% or
- 8.5V DC to 18V DC wide range input

Note: It is not possible to use E2 rated boards with wide range input!

Supply Voltage Ripple

- Maximum 100mV peak to peak 0-20 MHz

3.3.1 Supply Current (Windows XP SP2)

The tested boards were mounted on a Kontron Evaluation Board (Article number: 38100-0000-00-0), a mouse and a keyboard were connected. The Power-consumption tests were executed during Windows XP SP2 by using a tool to stress the CPU (100 % load). The power measurements values were acquired after 15 min full load and a stable CPU die temperature. To ensure a stable die temperature a corresponding heatsink was used to hold the temperature under the critical trip point.

All boards were equipped with DDR3 SDRAM. The Modules were tested using maximum CPU frequency.

Processor / board revision	MHz	RAM MB	Full Load			Idle		
			[A]12V	[A]5V_SB	[W]	[A]12V	[A]5V_SB	[W]
SP9300	2x2266	1024	3,14	0,06	**37,98**	0,64	0,06	**7,99**
SL9400	2x1866	1024	2,44	0,06	**29,58**	0,65	0,06	**8,13**
SU9300	2x1200	1024	1,40	0,06	**17,10**	0,62	0,06	**7,78**
CM722	1200	1024	1,09	0,06	**13,32**	0,63	0,06	**7,98**

Processor / board revision	MHz	RAM MB	Idle with Speedstep			Standby S1		
			[A]12V	[A]5V_SB	[W]	[A]12V	[A]5V_SB	[W]
SP9300	2x2266	1024	TBD	TBD		TBD	TBD	
SL9400	2x1866	1024	TBD	TBD		TBD	TBD	
SU9300	2x1200	1024	TBD	TBD		TBD	TBD	
CM722	1200	1024	TBD	TBD		TBD	TBD	

Processor / board revision	MHz	RAM MB	S3hot			S3cold		
			[A]12V	[A]5V_SB	[W]	[A]12V	[A]5V_SB	[W]
SP9300	2x2266	1024	TBD	TBD		TBD	TBD	
SL9400	2x1866	1024	TBD	TBD		TBD	TBD	
SU9300	2x1200	1024	TBD	TBD		TBD	TBD	
CM722	1200	1024	TBD	TBD		TBD	TBD	

Processor / board revision	MHz	RAM MB	Soft Off S5					
			[A]12V	[A]5V_SB	[W]			
SP9300	2x2266	1024	0,00	0,19	**0,95**			
SL9400	2x1866	1024	0,00	0,26	**1,30**			
SU9300	2x1200	1024	0,00	0,27	**1,37**			
CM722	1200	1024	0,00	0,26	**1,28**			

3.3.2 CMOS Battery Power Consumption

tbd

3.4 Environmental Specification

3.4.1 Temperature

Operating: (with Kontron Embedded Modules heat-spreader plate assembly):

- Ambient temperature: 0°C to 60°C
- Maximum heatspreader-plate temperature: 0°C to 60°C

Non-operating: -30°C to 85°C

Note: The maximum operating temperature with the heatspreader plate is the maximum measurable temperature on any spot on the heatspreader's surface. You must maintain the temperature according to the above specification.

Operating (without Kontron Embedded Modules heat-spreader plate assembly):

- Maximum operating temperature: 0°C to 60°C

Non operating: -30 to +85 °C

Note: The maximum operating temperature is the maximum measurable temperature on any spot on a module's surface. You must maintain the temperature according to the above specification.

3.4.2 Humidity

- Operating: 10% to 90% (non condensing)
- Non operating: 5% to 95% (non condensing)

3.5 MTBF

The following MTBF (Mean Time Between Failure) values were calculated using a combination of manufacturer's test data, if the data was available, and a Bellcore calculation for the remaining parts. The Bellcore calculation used is "Method 1 Case 1". In that particular method the components are assumed to be operating at a 50 % stress level in a 40° C ambient environment and the system is assumed to have not been burned in. Manufacturer's data has been used wherever possible. The manufacturer's data, when used, is specified at 50° C, so in that sense the following results are slightly conservative. The MTBF values shown below are for a 40° C in an office or telecommunications environment. Higher temperatures and other environmental stresses (extreme altitude, vibration, salt water exposure, etc.) lower MTBF values.

➤ System MTBF (hours) : 147066

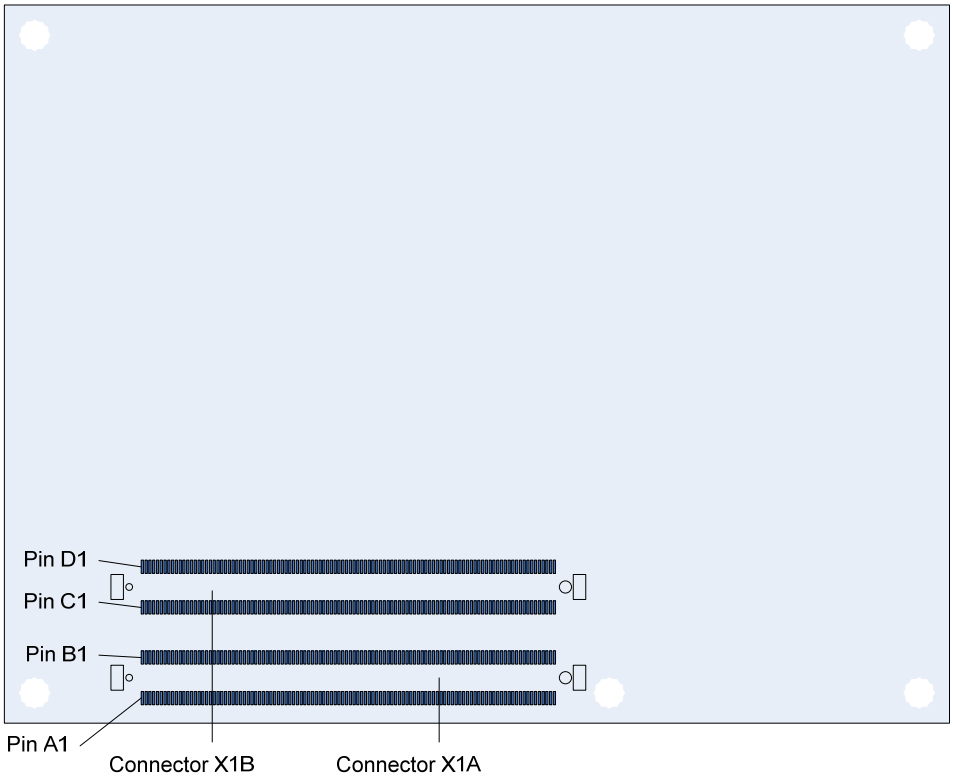
Notes: Fans usually shipped with Kontron Embedded Modules GmbH products have 50,000-hour typical operating life. The above estimates assume no fan, but a passive heat sinking arrangement.

4 Connector Pinouts

4.1 Connector Location

There are 2 connectors on the basic sized module. Connector X1A and Connector X1B are shown in the following drawing. It is a top layer view and the connectors are seen "through" the PCB.

Each connector consist s of 2 connector rows. Connector X1A has rows A and B and connector X1B has rows C and D.



4.2 Pinout Tables

Type	Description
I/O-3,3	Bi-directional 3,3 V IO-Signal
I/O-5T	Bi-dir. 3,3V I/O (5V Tolerance)
I/O-5	Bi-directional 5V I/O-Signal
I-3,3	3,3V Input
I/OD	Bi-directional Input/Output Open Drain
I-5T	3,3V Input (5V Tolerance)
OA	Output Analog
OD	Output Open Drain
O-1,8	1,8V Output
O-3,3	3,3V Output
O-5	5V Output
DP-I/O	Differential Pair Input/Output
DP-I	Differential Pair Input
DP-O	Differential Pair Output
PU	Pull-Up Resistor
PD	Pull-Down Resistor
PWR	Power Connection

Notes: To protect external power lines of peripheral devices, make sure that: the wires have the right diameter to withstand the maximum available current the enclosure of the peripheral device fulfils the fire-protection requirements of IEC/EN60950

4.3 Connector X1A

Connector X1A (Signal Levels A1-A55)

Pin A1-A55 [LAN | Power | USB | SATA | PCIe | AUDIO]

Pin	Signal	Description	Type	Termination	Comment
A1	GND	Power Ground	PWR	-	-
A2	GBE0_MDI3-	GBE0_MDI3_N | Ethernet Receive Data	DP-I	-	-
A3	GBE0_MDI3+	GBE0_MDI3_P | Ethernet Receive Data	DP-I	-	-
A4	GBE0_LINK10	GBE0_LINK100# | Ethernet Speed LED	O-3,3	-	-
A5	GBE0_LINK10	GBE0_LINK1000# | Ethernet Speed LED	O-3,3	-	-
A6	GBE0_MDI2-	GBE0_MDI2_N | Ethernet Receive Data	DP-I	-	-
A7	GBE0_MDI2+	GBE0_MDI2_P | Ethernet Receive Data	DP-I	-	-
A8	GBE0_LINK#	GBE0_LINK# | LAN Link LED	OD	-	-
A9	GBE0_MDI1-	GBE0_MDI1_N | Ethernet Receive Data	DP-I	-	-
A10	GBE0_MDI1+	GBE0_MDI1_P | Ethernet Receive Data	DP-I	-	-
A11	GND	Power Ground	PWR	-	-
A12	GBE0_MDI0-	GBE0_MDI0_N | Ethernet Transmit	DP-O	-	-
A13	GBE0_MDI0+	GBE0_MDI0_P | Ethernet Transmit Data	DP-O	-	-
A14	GBE0_CTREF	GBE0_CTREF	O-1,8	-	is on a power rail controlled by Intels ME
A15	SUS_S3#	PM_SLP_S3_EXT#	O-3,3	PU 10k 3,3V (S5)	-
A16	SATA0_TX+	SATA_TX0_P | SATA 0 Transmit Data +	DP-O	-	-
A17	SATA0_TX-	SATA_TX0_N | SATA 0 Transmit Data -	DP-O	-	-
A18	SUS_S4#	PM_SLP_S4_EXT#	O-3,3	-	-
A19	SATA0_RX+	SATA_RX0_P | SATA 0 Receive Data +	DP-I	-	-
A20	SATA0_RX-	SATA_RX0_N | SATA 0 Receive Data -	DP-I	-	-
A21	GND	Power Ground	PWR	-	-
A22	SATA2_TX+	SATA_TX2_P | SATA 2 Transmit Data +	DP-O	-	-
A23	SATA2_TX-	SATA_TX2_N | SATA 2 Transmit Data -	DP-O	-	-
A24	SUS_S5#	PM_SLP_S#5	O-3,3	-	-
A25	SATA2_RX+	SATA_RX2_P | SATA 2 Receive Data +	DP-I	-	-
A26	SATA2_RX-	SATA_RX2_N | SATA 2 Receive Data -	DP-I	-	-
A27	BATLOW#	PM_BATLOW# | Battery Low	I-3,3	PU 8k25 3,3V	-
A28	ATA_ACT#	ATA_LED# | SATA LED	O-3,3	PU 10k 3,3V (S0)	int. PU 15k in ICH9 only active if
A29	AC_SYNC	HDA_SYNC | HD Audio Sync	O-3,3	-	opt. for x4: PU 1k 3,3V(S0)
A30	AC_RST#	HDA_RST# | HD Audio Reset	O-3,3	-	int. PD 20k in ICH9
A31	GND	Power Ground	PWR	-	-
A32	AC_BITCLK	HDA_BITCLK | HD Audio Clock	O-3,3	-	int. PD 20k in ICH9 active only in S3
A33	AC_SDOUT	HDA_SDOUT | HD Audio Data	O-3,3	-	int. PD 20k in ICH9– x4 => PU 1k
A34	BIOS_DISABLE	BIOS_DISABLE#	I-3,3	-	-
A35	THRMTRIP#	EXT_THRMTRIP#	I/O-	PU 10k 3,3V (S0)	-
A36	USB6-	USB6_N | USB Data – Port6	DP-I/O	-	int. PD 15k in ICH9 | 5V tolerant
A37	USB6+	USB6_P | USB Data + Port6	DP-I/O	-	int. PD 15k in ICH9 | 5V tolerant
A38	USB_6_7_OC#	USB_67_OC# | USB OverCurrent Port	I-3,3	PU 10k 3,3V (S5)	-
A39	USB4-	USB4_N | USB Data - Port4	DP-I/O	-	int. PD 15k in ICH9 | 5V tolerant
A40	USB4+	USB4_P | USB Data + Port4	DP-I/O	-	int. PD 15k in ICH9 | 5V tolerant
A41	GND	Power Ground	PWR	-	-
A42	USB2-	USB2_N | USB Data - Port2	DP-I/O	-	int. PD 15k in ICH9 | 5V tolerant
A43	USB2+	USB2_P | USB Data + Port2	DP-I/O	-	int. PD 15k in ICH9 | 5V tolerant
A44	USB_2_3_OC#	USB_23_OC# | USB OverCurrent Port	I-3,3	PU 10k 3,3V (S5)	-
A45	USB0-	USB0_N | USB Data - Port0	DP-I/O	-	int. PD 15k in ICH9 | 5V tolerant
A46	USB0+	USB0_P | USB Data + Port0	DP-I/O	-	int. PD 15k in ICH9 | 5V tolerant
A47	VCC_RTC	V_BAT	PWR	-	-
A48	EXCD0_PERST#	EXCD0_PERST#| Express card reset	O-3,3	-	-
A49	EXCD0_CPPE#	EXCD0_CPPE#| capable c. request	I-3,3	PU 10k 3,3V (S5)	-
A50	LPC_SERIRQ	LPC_SERIRQ | Serial Interrupt Request	IO-3,3	PU 10k 3,3V (S0)	-
A51	GND	Power Ground	PWR	-	-
A52	PCIE_TX5+	*opt. PCI Express lane 5 + Transmit*	Nc	-	just available if no GbEthernet PHY is
A53	PCIE_TX5-	*opt. PCI Express lane 5 - Transmit*	Nc	-	just available if no GbEthernet PHY is
A54	GPI0	EXT_GPI0 | General Purpose Input 0	I-3,3	PU 10k 3,3V (S0)	-
A55	PCIE_TX4+	PCI Express lane 4 + Transmit	DP-O	-	-

Note: The termination resistors in this table are already mounted on the ETXexpress® board. Refer to the design guide for information about additional termination resistors.

Connector X1A (Signal Levels A56-A110)

Pin A56-A110

[Power | LVDS | PCIe]

Pin	Signal	Description	Type	Termination	Comment
A56	PCIE_TX4-	PCI Express lane 4 - Transmit	DP-O	-	-
A57	GND	Power Ground	PWR	-	-
A58	PCIE_TX3+	PCI Express lane 3 + Transmit	DP-O	-	-
A59	PCIE_TX3-	PCI Express lane 3 - Transmit	DP-O	-	-
A60	GND	Power Ground	PWR	-	-
A61	PCIE_TX2+	PCI Express lane 2 + Transmit	DP-O	-	-
A62	PCIE_TX2-	PCI Express lane 2 - Transmit	DP-O	-	-
A63	GPI1	EXT_GPI1 | General Purpose Input 1	I-3,3	PU 10k 3,3V (S0)	-
A64	PCIE_TX1+	PCI Express lane 1 + Transmit	DP-O	-	-
A65	PCIE_TX1-	PCI Express lane 1 - Transmit	DP-O	-	-
A66	GND	Power Ground	PWR	-	-
A67	GPI2	EXT_GPI2 | General Purpose Input 2	I-3,3	PU 10k 3,3V (S0)	-
A68	PCIE_TX0+	PCI Express lane 0 + Transmit	DP-O	-	-
A69	PCIE_TX0-	PCI Express lane 0 - Transmit	DP-O	-	-
A70	GND	Power Ground	PWR	-	-
A71	LVDS_A0+	LVDS_A_DATA0_P | LVDS Channel A	DP-O	-	-
A72	LVDS_A0-	LVDS_A_DATA0_N | LVDS Channel A	DP-O	-	-
A73	LVDS_A1+	LVDS_A_DATA1_P | LVDS Channel A	DP-O	-	-
A74	LVDS_A1-	LVDS_A_DATA1_N | LVDS Channel A	DP-O	-	-
A75	LVDS_A2+	LVDS_A_DATA2_P| LVDS Channel A	DP-O	-	-
A76	LVDS_A2-	LVDS_A_DATA2_N | LVDS Channel A Data2	DP-O	-	-
A77	LVDS_VDD_EN	LVDS_VDD_EN | LVDS Panel Power Control	O-3,3	PD 100k	-
A78	LVDS_A3+	LVDS_A_DATA3_P | LVDS Channel A	DP-O	-	-
A79	LVDS_A3-	LVDS_A_DATA3_N | LVDS Channel A	DP-O	-	-
A80	GND	Power Ground	PWR	-	-
A81	LVDS_A_CK+	LVDS_A_CLK_P | LVDS Channel A Clock+	DP-O	-	-
A82	LVDS_A_CK-	LVDS_A_CLK_N | LVDS Channel A Clock-	DP-O	-	-
A83	LVDS_I2C_CK	LVDS_DDC_CLK | JILI I2C Clock	I/O-3,3	PU 2k21 3,3V (s0)	-
A84	LVDS_I2C_DAT	LVDS_DDC_DATA | JILI I2C Data	I/O-3,3	PU 2k21 3,3V (s0)	-
A85	GPI3	EXT_GPI3 | General Purpose Input 3	I-3,3	PU 10k 3,3V (S0)	-
A86	KBD_RST#	KBD_RST# | Keyboard Reset	I-3,3	PU 10k 3,3V (S0)	-
A87	KBD_A20GATE	KBD_A20GATE	I-3,3	PU 10k 3,3V (S0)	-
A88	PCIE0_CK_REF+	CLK_PCIE_CON_P	DP-O	-	-
A89	PCIE0_CK_REF-	CLK_PCIE_CON_N	DP-O	-	-
A90	GND	Power Ground	PWR	-	-
A91	RSVD	n.c.	Nc	-	-
A92	RSVD	n.c.	Nc	-	-
A93	GPO0	EXT_GPO0 | General Purpose Output 0	O-3,3	PD 10k	-
A94	RSVD	n.c.	Nc	-	-
A95	RSVD	n.c.	Nc	-	
A96	GND	Power Ground	PWR	-	-
A97	VCC_12V	12V VCC	PWR	-	-
A98	VCC_12V	12V VCC	PWR	-	-
A99	VCC_12V	12V VCC	PWR	-	-
A100	GND	Power Ground	PWR	-	-
A101	VCC_12V	12V VCC	PWR	-	-
A102	VCC_12V	12V VCC	PWR	-	-
A103	VCC_12V	12V VCC	PWR	-	-
A104	VCC_12V	12V VCC	PWR	-	-
A105	VCC_12V	12V VCC	PWR	-	-
A106	VCC_12V	12V VCC	PWR	-	-
A107	VCC_12V	12V VCC	PWR	-	-
A108	VCC_12V	12V VCC	PWR	-	-
A109	VCC_12V	12V VCC	PWR	-	-
A110	GND	Power Ground	PWR	-	-

Note: The termination resistors in this table are already mounted on the ETXexpress® board. Refer to the design guide for information about additional termination resistors.

Connector X1A (Signal Levels B1-B55)

Pin B1-B55 [LAN | Power | USB | SATA | PCIe | AUDIO | LPC]

Pin	Signal	Description	Type	Termination	Comment
B1	GND	Power Ground	PWR	-	-
B2	GBE0_ACT	GBE0_ACT# | Ethernet Activity LED	OD	-	-
B3	LPC_FRAME#	LPC_FRAME# | LPC Frame Indicator	I-3,3	-	-
B4	LPC_AD0	LPC_AD0 | LPC Adress & DATA Bus	I/O-3,3	-	int. PU 20k in ICH9
B5	LPC_AD1	LPC_AD1 | LPC Adress & DATA Bus	I/O-3,3	-	int. PU 20k in ICH9
B6	LPC_AD2	LPC_AD2 | LPC Adress & DATA Bus	I/O-3,3	-	int. PU 20k in ICH9
B7	LPC_AD3	LPC_AD3 | LPC Adress & DATA Bus	I/O-3,3	-	int. PU 20k in ICH9
B8	LPC_DRQ0#	LPC_DRQ#0 | LPC Request 0	I-3,3	PU 10k 3,3V	int. PU 20k in ICH9
B9	LPC_DRQ1#	LPC_DRQ#1 | LPC Request 1	I-3,3	PU 10k 3,3V	int. PU 20k in ICH10
B10	LPC_CLK	CLK_LPC_33M_EXT | 33MHz LPC clock	O-3,3	-	-
B11	GND	Power Ground	PWR	-	-
B12	PWRBTN#	EXT_PWRBTN# | Power Button	I-3,3	PU 20k 3,3V	-
B13	SMB_CK	SMB_CLK_EXT | SMBUS Clock	O-3,3	PU 2k2 3,3V	-
B14	SMB_DAT	SMB_DATA_EXT | SMBUS Data	IO-3,3	PU 2k2 3,3V	-
B15	SMB_ALERT#	SMB_ALERT# | SMBUS Interrupt	IO-3,3	PU 1k0 3,3V	-
B16	SATA1_TX+	SATA_TX1_P | SATA 1 Transmit Data +	DP-O	-	-
B17	SATA1_TX-	SATA_TX1_N | SATA 1 Transmit Data -	DP-O	-	-
B18	SUS_STAT#	PM_SUS_ STAT#	O-3,3	-	-
B19	SATA1_RX+	SATA_RX1_P | SATA 1 Receive Data +	DP-I	-	-
B20	SATA1_RX-	SATA_RX1_N | SATA 1 Receive Data -	DP-I	-	-
B21	GND	Power Ground	PWR	-	-
B22	SATA3_TX+	SATA_TX3_P | SATA 3 Transmit Data +	DP-O	-	-
B23	SATA3_TX-	SATA_TX3_N | SATA 3 Transmit Data -	DP-O	-	-
B24	PWR_OK	EXT_PWR_OK | Power OK	I-3,3	-	-
B25	SATA3_RX+	SATA_RX3_P | SATA 3 Receive Data +	DP-I	-	-
B26	SATA3_RX-	SATA_RX3_N | SATA 3 Receive Data -	DP-I	-	-
B27	WDT	WDT | Watch Dog Timer	O-3,3	-	-
B28	AC_SDIN2	HDA_SDIN2_ICH| HD Audio Serial Input	I-3,3	-	int. PD 20k in ICH9
B29	AC_SDIN1	HDA_SDIN1_ICH| HD Audio Serial Input	I-3,3	-	int. PD 20k in ICH9
B30	AC_SDIN0	HDA_SDIN0_ICH| HD Audio Serial Input	I-3,3	-	int. PD 20k in ICH9
B31	GND	Power Ground	PWR	-	-
B32	SPKR	HDA_SPKR | Speaker	O-3,3	-	int. PD 20k in ICH9
B33	I2C_CK	I2C_CLK_EXT | I2C clock	O-3,3	PU 2k21 3,3V	-
B34	I2C_DAT	I2C_DATA_EXT | I2C data	I/O-3,3	PU 2k21 3,3V	-
B35	THRM#	PM_THRM# | Over Temperature	O-3,3	PU 8k25 3,3V	-
B36	USB7-	USB7_N | USB Data – Port7	DP-I/O	-	int. PD 15k in ICH9 | 5V
B37	USB7+	USB7_P | USB Data + Port7	DP-I/O	-	int. PD 15k in ICH9 | 5V
B38	USB_4_5_OC#	USB_45_OC# | USB OverCurrent Port 4/5	I-3,3	PU 10k 3,3V	-
B39	USB5-	USB5_N | USB Data – Port5	DP-I/O	-	int. PD 15k in ICH9 | 5V
B40	USB5+	USB5_P | USB Data + Port5	DP-I/O	-	int. PD 15k in ICH9 | 5V
B41	GND	Power Ground	PWR	-	-
B42	USB3-	USB3_N | USB Data – Port3	DP-I/O	-	int. PD 15k in ICH9 | 5V
B43	USB3+	USB3_P | USB Data + Port3	DP-I/O	-	int. PD 15k in ICH9 | 5V
B44	USB_0_1_OC#	USB_01_OC# | USB OverCurrent Port 0/1	I-3,3	PU 10k 3,3V	-
B45	USB1-	USB1_N | USB Data – Port1	DP-I/O	-	int. PD 15k in ICH9 | 5V
B46	USB1+	USB1_P | USB Data + Port1	DP-I/O	-	int. PD 15k in ICH9 | 5V
B47	EXCD1_PERST#	EXCD1_PERST# | Express card reset	O-3,3	-	-
B48	EXCD1_CPPE#	EXCD1_CPPE# | capable c. request	I-3,3	PU 10k 3,3V	-
B49	SYS_RESET#	EXT_SYS_RESET# | Reset Input	I-3,3	PU 10k 3,3V	-
B50	CB_RESET#	CB_RESET# | Carrier board Reset	O-3,3	-	-
B51	GND	Power Ground	PWR	-	-
B52	PCIE_RX5+	*opt. PCI Express lane 5 + Recieve*	Nc	-	just available if no
B53	PCIE_RX5-	*opt. PCI Express lane 5 - Recieve*	Nc	-	just available if no
B54	GPO1	EXT_GPO1 | General Purpose Output 1	O-3,3	PD 10k	-
B55	PCIE_RX4+	PCI Express lane 4 + Recieve	DP-I	-	availlable when ICH9-MDH or

Note: The termination resistors in this table are already mounted on the ETXexpress® board. Refer to the design guide for information about additional termination resistors.

Connector X1A (Signal Levels B56-B110)

Pin B56-B110 [Power | PCIe | LVDS | CRT,TV]

Pin	Signal	Description	Type	Termination	Comment
B56	PCIE_RX4-	PCI Express lane 4 - Recieve	DP-I	-	availlable when ICH9-MDH or
B57	GPO2	EXT_GPO2 | General Purpose Output 2	O-3,3	PD 10k	
B58	PCIE_RX3+	PCI Express lane 3 + Recieve	DP-I	-	availlable when ICH9-MDH or
B59	PCIE_RX3-	PCI Express lane 3 - Recieve	DP-I	-	availlable when ICH9-MDH or
B60	GND	Power Ground	PWR	-	-
B61	PCIE_RX2+	PCI Express lane 2 + Recieve	DP-I	-	-
B62	PCIE_RX2-	PCI Express lane 2 - Recieve	DP-I	-	-
B63	GPO3	EXT_GPO3 | General Purpose Output 3	O-3,3	PD 10k	-
B64	PCIE_RX1+	PCI Express lane 1 + Recieve	DP-I	-	-
B65	PCIE_RX1-	PCI Express lane 1 - Recieve	DP-I	-	-
B66	WAKE0#	PCIE_WAKE#	IO-3,3	PU 1k0 3,3V	-
B67	WAKE1#	WAKE1#	I-3,3	PU 10k 3,3V	-
B68	PCIE_RX0+	PCI Express lane 0 + Recieve	DP-I	-	-
B69	PCIE_RX0-	PCI Express lane 0 - Recieve	DP-I	-	-
B70	GND	Power Ground	PWR	-	-
B71	LVDS_B0+	LVDS_B_DATA0_P | LVDS Channel B Data0+	DP-O	-	-
B72	LVDS_B0-	LVDS_B_DATA0_N | LVDS Channel B Data0-	DP-O	-	-
B73	LVDS_B1+	LVDS_B_DATA1_P | LVDS Channel B Data1+	DP-O	-	-
B74	LVDS_B1-	LVDS_B_DATA1_N | LVDS Channel B Data1-	DP-O	-	-
B75	LVDS_B2+	LVDS_B_DATA2_P| LVDS Channel B Data2+	DP-O	-	-
B76	LVDS_B2-	LVDS_B_DATA2_N | LVDS Channel B Data2	DP-O	-	-
B77	LVDS_B3+	LVDS_B_DATA3_P | LVDS Channel B Data3+	DP-O	-	-
B78	LVDS_B3-	LVDS_B_DATA3_N | LVDS Channel B Data3-	DP-O	-	-
B79	LVDS_BKLT_EN	LVDS_BKLT_CTRL | Panel Backlight ON	O-3,3	PD 100k	-
B80	GND	Power Ground	PWR	-	-
B81	LVDS_B_CK+	LVDS_B_CLK_P | LVDS Channel B Clock+	DP-O	-	-
B82	LVDS_B_CK-	LVDS_B_CLK_N | LVDS Channel B Clock-	DP-O	-	-
B83	LVDS_BKLT_CTRL	LVDS_BKLT_CTRL | Backlight Brightness	O-3,3	-	-
B84	VCC_5V_SBY	+V_STBY_ETX | 5V Standby	PWR 5V	-	-
B85	VCC_5V_SBY	+V_STBY_ETX | 5V Standby	PWR 5V	-	-
B86	VCC_5V_SBY	+V_STBY_ETX | 5V Standby	PWR 5V	-	-
B87	VCC_5V_SBY	+V_STBY_ETX | 5V Standby	PWR 5V	-	-
B88	RSVD	n.c.	nc	-	-
B89	VGA_RED	CRT_RED | Analog Video RGB-RED	OA	PD 150R	-
B90	GND	Power Ground	PWR	-	-
B91	VGA_GRN	CRT_GREEN | Analog Video RGB-GREEN	OA	PD 150R	-
B92	VGA_BLU	CRT_BLUE | Analog Video RGB-BLUE	OA	PD 150R	-
B93	VGA_HSYNC	CRT_HSYNC | Analog Video H-Sync	O-3,3	-	-
B94	VGA_VSYNC	CRT_VSYNC | Analog Video V-Sync	O-3,3	-	-
B95	VGA_I2C_CK	CRT_DDC_CLK | Display Data Channel Clock	I/O-5	PU 2k21 5V (S0)	-
B96	VGA_I2C_DAT	CRT_DDC_DATA | Display Data Channel Data	I/O-5	PU 2k21 5V (S0)	-
B97	TV_DAC_A	TV_DACA_CVBS | Composite CVBS	OA	PD 150R	-
B98	TV_DAC_B	TV_DADB_Y | TV Luminance Signal	OA	PD 150R	-
B99	TV_DAC_C	TV_DADC_C | TV Chrominance Signal	OA	PD 150R	-
B100	GND	Power Ground	PWR	-	-
B101	VCC_12V	12V VCC	PWR	-	-
B102	VCC_12V	12V VCC	PWR	-	-
B103	VCC_12V	12V VCC	PWR	-	-
B104	VCC_12V	12V VCC	PWR	-	-
B105	VCC_12V	12V VCC	PWR	-	-
B106	VCC_12V	12V VCC	PWR	-	-
B107	VCC_12V	12V VCC	PWR	-	-
B108	VCC_12V	12V VCC	PWR	-	-
B109	VCC_12V	12V VCC	PWR	-	-
B110	GND	Power Ground	PWR	-	-

Note: The termination resistors in this table are already mounted on the ETXexpress® board. Refer to the design guide for information about additional termination resistors.

4.4 Connector X1B

Connector X1B (Signal Levels C1-C55)

Pin C1-C55 [IDE | Power | USB | SATA | PCIe | AUDIO]

Pin	Signal	Description	Type	Termination	Comment
C1	GND	Power Ground	PWR	-	-
C2	IDE_D7	IDE Data Bus	I/O-5T	PD 10k	-
C3	IDE_D6	IDE Data Bus	I/O-5T	-	-
C4	IDE_D3	IDE Data Bus	I/O-5T	-	-
C5	IDE_D15	IDE Data Bus	I/O-5T	-	-
C6	IDE_D8	IDE Data Bus	I/O-5T	-	-
C7	IDE_D9	IDE Data Bus	I/O-5T	-	-
C8	IDE_D2	IDE Data Bus	I/O-5T	-	-
C9	IDE_D13	IDE Data Bus	I/O-5T	-	-
C10	IDE_D1	IDE Data Bus	I/O-5T	-	-
C11	GND	Power Ground	PWR	-	-
C12	IDE_D14	IDE Data Bus	I/O-5T	-	-
C13	IDE_IORDY	IDE I/O Ready	I/O-5T	PU 4k7 3,3V (S0)	-
C14	IDE_IOR#	IDE I/O Read	I/O-3,3	-	-
C15	PCI_PME#	PCI Power Management Event	I/O-3,3	-	int. PU 20k in ICH9
C16	PCI_GNT2#	PCI Bus Grant 2	O-3,3	-	int. PU 20k in ICH9 (if
C17	PCI_REQ2#	PCI Bus Request 2	I-5T	PU 8k2 3,3V (S0)	-
C18	PCI_GNT1#	PCI Bus Grant 1	O-3,3	-	int. PU 20k in ICH9 (if
C19	PCI_REQ1#	PCI Bus Request 1	I-5T	PU 8k2 3,3V (S0)	-
C20	PCI_GNT0#	PCI Bus Grant 0	O-3,3	PD 1k0	int. PU 20k in ICH9 (if
C21	GND	Power Ground	PWR	-	-
C22	PCI_REQ0#	PCI Bus Reqest 0	I-5T	PU 8k2 3,3V (S0)	-
C23	PCI_RST#	PCI Bus Reset	O-3,3	-	-
C24	PCI_AD0	PCI Adress & Data Bus line	I/O-5T	-	-
C25	PCI_AD2	PCI Adress & Data Bus line	I/O-5T	-	-
C26	PCI_AD4	PCI Adress & Data Bus line	I/O-5T	-	-
C27	PCI_AD6	PCI Adress & Data Bus line	I/O-5T	-	-
C28	PCI_AD8	PCI Adress & Data Bus line	I/O-5T	-	-
C29	PCI_AD10	PCI Adress & Data Bus line	I/O-5T	-	-
C30	PCI_AD12	PCI Adress & Data Bus line	I/O-5T	-	-
C31	GND	Power Ground	PWR	-	-
C32	PCI_AD14	PCI Adress & Data Bus line	I/O-5T	-	-
C33	PCI_C/BE1#	PCI Bus Command and Byte enables 1	I/O-5T	-	-
C34	PCI_PERR#	PCI Bus Grant Error	I/O-5T	PU 8k2 3,3V (S0)	-
C35	PCI_LOCK#	PCI Bus Lock	I/O-5T	PU 8k2 3,3V (S0)	-
C36	PCI_DEVSEL#	PCI Bus Device Select	I/O-5T	PU 8k2 3,3V (S0)	-
C37	PCI_IRDY#	PCI Bus Bus Initiator Ready	I/O-5T	PU 8k2 3,3V (S0)	-
C38	PCI_C/BE2#	PCI Bus Command and Byte enables 2	I/O-5T	-	-
C39	PCI_AD17	PCI Adress & Data Bus line	I/O-5T	-	-
C40	PCI_AD19	PCI Adress & Data Bus line	I/O-5T	-	-
C41	GND	Power Ground	PWR	-	-
C42	PCI_AD21	PCI Adress & Data Bus line	I/O-5T	-	-
C43	PCI_AD23	PCI Adress & Data Bus line	I/O-5T	-	-
C44	PCI_C/BE3#	PCI Bus Command and Byte enables 3	I/O-5T	-	-
C45	PCI_AD25	PCI Adress & Data Bus line	I/O-5T	-	-
C46	PCI_AD27	PCI Adress & Data Bus line	I/O-5T	-	-
C47	PCI_AD29	PCI Adress & Data Bus line	I/O-5T	-	-
C48	PCI_AD31	PCI Adress & Data Bus line	I/O-5T	-	-
C49	PCI_IRQA#	PCI Bus Interrupt Request A	I-5T	PU 8k2 3,3V (S0)	-
C50	PCI_IRQB#	PCI Bus Interrupt Request B	I-5T	PU 8k2 3,3V (S0)	-
C51	GND	Power Ground	PWR	-	-
C52	PEG_RX0+	PCIexpress Graphics Recieve + (0)	DP-I	-	-
C53	PEG_RX0-	PCIexpress Graphics Recieve - (0)	DP-I	-	-
C54	TYPE0#	n.c. for type 2 module	nc	-	-
C55	PEG_RX1+	PCIexpress Graphics Recieve + (1)	DP-I	-	-

Note: The termination resistors in this table are already mounted on the ETXexpress® board. Refer to the design guide for information about additional termination resistors.

Connector X1B (Signal Levels C56-C110)

Pin C56-C110

[Power | LVDS | PCIe]

Pin	Signal	Description	Type	Termination	Comment
C56	PEG_RX1-	PCIexpress Graphics Recieve - (1)	DP-I	-	-
C57	TYPE1#	n.c. for type 2 module	nc	-	-
C58	PEG_RX2+	PCIexpress Graphics Recieve + (2)	DP-I	-	-
C59	PEG_RX2-	PCIexpress Graphics Recieve - (2)	DP-I	-	-
C60	GND	Power Ground	PWR	-	-
C61	PEG_RX3+	PCIexpress Graphics Recieve + (3)	DP-I	-	-
C62	PEG_RX3-	PCIexpress Graphics Recieve - (3)	DP-I	-	-
C63	RSVD	n.c.	nc	-	-
C64	RSVD	n.c.	nc	-	-
C65	PEG_RX4+	PCIexpress Graphics Recieve + (4)	DP-I	-	-
C66	PEG_RX4-	PCIexpress Graphics Recieve - (4)	DP-I	-	-
C67	RSVD	n.c.	nc	-	-
C68	PEG_RX5+	PCIexpress Graphics Recieve + (5)	DP-I	-	-
C69	PEG_RX5-	PCIexpress Graphics Recieve - (5)	DP-I	-	-
C70	GND	Power Ground	PWR	-	-
C71	PEG_RX6+	PCIexpress Graphics Recieve + (6)	DP-I	-	-
C72	PEG_RX6-	PCIexpress Graphics Recieve - (6)	DP-I	-	-
C73	SDVO_DATA	SDVO_CTRLDATA	I/O-3,3	-	opt. PU 2k21 3,3V (S0) =
C74	PEG_RX7+	PCIexpress Graphics Recieve + (7)	DP-I	-	-
C75	PEG_RX7-	PCIexpress Graphics Recieve - (7)	DP-I	-	-
C76	GND	Power Ground	PWR	-	-
C77	RSVD	n.c.	nc	-	-
C78	PEG_RX8+	PCIexpress Graphics Recieve + (8)	DP-I	-	-
C79	PEG_RX8-	PCIexpress Graphics Recieve - (8)	DP-I	-	-
C80	GND	Power Ground	PWR	-	-
C81	PEG_RX9+	PCIexpress Graphics Recieve + (9)	DP-I	-	-
C82	PEG_RX9-	PCIexpress Graphics Recieve - (9)	DP-I	-	-
C83	RSVD	n.c.	nc	-	-
C84	GND	Power Ground	PWR	-	-
C85	PEG_RX10+	PCIexpress Graphics Recieve + (10)	DP-I	-	-
C86	PEG_RX10-	PCIexpress Graphics Recieve - (10)	DP-I	-	-
C87	GND	Power Ground	PWR	-	-
C88	PEG_RX11+	PCIexpress Graphics Recieve + (11)	DP-I	-	-
C89	PEG_RX11-	PCIexpress Graphics Recieve – (11)	DP-I	-	-
C90	GND	Power Ground	PWR	-	-
C91	PEG_RX12+	PCIexpress Graphics Recieve + (12)	DP-I	-	-
C92	PEG_RX12-	PCIexpress Graphics Recieve - (12)	DP-I	-	-
C93	GND	Power Ground	PWR	-	-
C94	PEG_RX13+	PCIexpress Graphics Recieve + (13)	DP-I	-	-
C95	PEG_RX13-	PCIexpress Graphics Recieve - (13)	DP-I	-	-
C96	GND	Power Ground	PWR	-	-
C97	RSVD	n.c.	nc	-	-
C98	PEG_RX14+	PCIexpress Graphics Recieve + (14)	DP-I	-	-
C99	PEG_RX14-	PCIexpress Graphics Recieve - (14)	DP-I	-	-
C100	GND	Power Ground	PWR	-	-
C101	PEG_RX15+	PCIexpress Graphics Recieve + (15)	DP-I	-	-
C102	PEG_RX15-	PCIexpress Graphics Recieve - (15)	DP-I	-	-
C103	GND	Power Ground	PWR	-	-
C104	VCC_12V	12V VCC	PWR	-	-
C105	VCC_12V	12V VCC	PWR	-	-
C106	VCC_12V	12V VCC	PWR	-	-
C107	VCC_12V	12V VCC	PWR	-	-
C108	VCC_12V	12V VCC	PWR	-	-
C109	VCC_12V	12V VCC	PWR	-	-
C110	GND	Power Ground	PWR	-	-

Note: The termination resistors in this table are already mounted on the ETXexpress® board. Refer to the design guide for information about additional termination resistors.

Connector X1B (Signal Levels D1-D55)

Pin D1-D55 [IDE | Power | USB | SATA | PCIe | AUDIO | LPC]

Pin	Signal	Description	Type	Termination	Comment
D1	GND	Power Ground	PWR	-	-
D2	IDE_D5	IDE Data Bus	I/O-5T	-	-
D3	IDE_D10	IDE Data Bus	I/O-5T	-	-
D4	IDE_D11	IDE Data Bus	I/O-5T	-	-
D5	IDE_D12	IDE Data Bus	I/O-5T	-	-
D6	IDE_D4	IDE Data Bus	I/O-5T	-	-
D7	IDE_D0	IDE Data Bus	I/O-5T	-	-
D8	IDE_REQ	IDE Data Bus	I/O-5T	PD 5k62	-
D9	IDE_IOW#	IDE IO Write	O-3,3	-	-
D10	IDE_ACK#	IDE DMA Acknowledge	O-3,3	-	-
D11	GND	Power Ground	PWR	-	-
D12	IDE_IRQ	IDE Interrupt Request	I-5T	PD 10k	-
D13	IDE_A0	IDE Adress Bus	O-3,3	-	-
D14	IDE_A1	IDE Adress Bus	O-3,3	-	-
D15	IDE_A2	IDE Adress Bus	O-3,3	-	-
D16	IDE_CS1#	IDE Chip Select Channel 0	O-3,3	-	-
D17	IDE_CS3#	IDE Chip Select Channel 1	O-3,3	-	-
D18	IDE_RESET#	IDE Hard Drive Reset	O-3,3	-	int. PU 31k in PATA bridge |
D19	PCI_GNT3#	PCI Bus Grant 3	O-3,3	-	int. PU 20k in ICH9 (if
D20	PCI_REQ3#	PCI Bus Reqest 0	I-5T	PU 8k2 3,3V	-
D21	GND	Power Ground	PWR	-	-
D22	PCI_AD1	PCI Adress & Data Bus line	I/O-5T	-	-
D23	PCI_AD3	PCI Adress & Data Bus line	I/O-5T	-	-
D24	PCI_AD5	PCI Adress & Data Bus line	I/O-5T	-	-
D25	PCI_AD7	PCI Adress & Data Bus line	I/O-5T	-	-
D26	PCI_C/BE0#	PCI Bus Command and Byte enables 0	I/O-5T	-	-
D27	PCI_AD9	PCI Adress & Data Bus line	I/O-5T	-	-
D28	PCI_AD11	PCI Adress & Data Bus line	I/O-5T	-	-
D29	PCI_AD13	PCI Adress & Data Bus line	I/O-5T	-	-
D30	PCI_AD15	PCI Adress & Data Bus line	I/O-5T	-	-
D31	GND	Power Ground	PWR	-	-
D32	PCI_PAR	PCI Bus Parity	I/O-5T	-	-
D33	PCI_SERR#	PCI Bus System Error	I/O-5T	PU 8k2 3,3V	-
D34	PCI_STOP#	PCI Bus Stop	I/O-5T	PU 8k2 3,3V	-
D35	PCI_TRDY#	PCI Bus Target Ready	I/O-5T	PU 8k2 3,3V	-
D36	PCI_FRAME#	PCI Bus Cycle Frame	I/O-5T	PU 8k2 3,3V	-
D37	PCI_AD16	PCI Adress & Data Bus line	I/O-5T	-	-
D38	PCI_AD18	PCI Adress & Data Bus line	I/O-5T	-	-
D39	PCI_AD20	PCI Adress & Data Bus line	I/O-5T	-	-
D40	PCI_AD22	PCI Adress & Data Bus line	I/O-5T	-	-
D41	GND	Power Ground	PWR	-	-
D42	PCI_AD24	PCI Adress & Data Bus line	I/O-5T	-	-
D43	PCI_AD26	PCI Adress & Data Bus line	I/O-5T	-	-
D44	PCI_AD28	PCI Adress & Data Bus line	I/O-5T	-	-
D45	PCI_AD30	PCI Adress & Data Bus line	I/O-5T	-	-
D46	PCI_IRQC#	PCI Bus Interrupt Request C	I-5T	PU 8k2 3,3V	-
D47	PCI_IRQD#	PCI Bus Interrupt Request D	I-5T	PU 8k2 3,3V	-
D48	PCI_CLKRUN#	PCI Clock Run	I-5T	PU 8k25 3,3V	-
D49	PCI_M66EN	n.c.	nc	-	-
D50	PCI_CLK	CLK_PCI_33M_EXT | PCI Clock 33MHz	O-3,3	-	-
D51	GND	Power Ground	PWR	-	-
D52	PEG_TX0+	PCIexpress Graphics Transmit + (0)	DP-O	-	-
D53	PEG_TX0-	PCIexpress Graphics Transmit - (0)	DP-O	-	-
D54	PEG_LANE_RV#	PCIexpress Graphics Lane Reversal	I-3,3	-	-
D55	PEG_TX1+	PCIexpress Graphics Transmit + (1)	DP-O	-	-

Note: The termination resistors in this table are already mounted on the ETXexpress® board. Refer to the design guide for information about additional termination resistors.

Connector X1B (Signal Levels D56-D110)

Pin D56-D110 [IDE | Power | USB | SATA | PCIe | AUDIO | LPC]

Pin	Signal	Description	Type	Termination	Comment
D56	PEG_TX1-	PCIexpress Graphics Transmit - (1)	DP-O	-	-
D57	TYPE2#	n.c. for type 2 module	nc	-	-
D58	PEG_TX2+	PCIexpress Graphics Transmit + (2)	DP-O	-	-
D59	PEG_TX2-	PCIexpress Graphics Transmit - (2)	DP-O	-	-
D60	GND	Power Ground	PWR	-	-
D61	PEG_TX3+	PCIexpress Graphics Transmit + (3)	DP-O	-	-
D62	PEG_TX3-	PCIexpress Graphics Transmit - (3)	DP-O	-	-
D63	RSVD	-	nc	-	
D64	RSVD	-	nc	-	
D65	PEG_TX4+	PCIexpress Graphics Transmit + (4)	DP-O	-	-
D66	PEG_TX4-	PCIexpress Graphics Transmit - (4)	DP-O	-	-
D67	GND	Power Ground	PWR	-	-
D68	PEG_TX5+	PCIexpress Graphics Transmit + (5)	DP-O	-	-
D69	PEG_TX5-	PCIexpress Graphics Transmit - (5)	DP-O	-	-
D70	GND	Power Ground	PWR	-	-
D71	PEG_TX6+	PCIexpress Graphics Transmit + (6)	DP-O	-	-
D72	PEG_TX6-	PCIexpress Graphics Transmit - (6)	DP-O	-	-
D73	SDVO_CLK	SDVO_CTRLCLK	IO-3,3	-	-
D74	PEG_TX7+	PCIexpress Graphics Transmit + (7)	DP-O	-	-
D75	PEG_TX7-	PCIexpress Graphics Transmit - (7)	DP-O	-	-
D76	GND	Power Ground	PWR	-	-
D77	IDE_CBLID	IDE_CBLID# | IDE cable type detect	I/O-3,3	-	opt. int. PU in IDE flash
D78	PEG_TX8+	PCIexpress Graphics Transmit + (8)	DP-O	-	-
D79	PEG_TX8-	PCIexpress Graphics Transmit - (8)	DP-O	-	-
D80	GND	Power Ground	PWR	-	-
D81	PEG_TX9+	PCIexpress Graphics Transmit + (9)	DP-O	-	-
D82	PEG_TX9-	PCIexpress Graphics Transmit - (9)	DP-O	-	-
D83	RSVD	n.c.	nc	-	-
D84	GND	Power Ground	PWR	-	-
D85	PEG_TX10+	PCIexpress Graphics Transmit + (10)	DP-O	-	-
D86	PEG_TX10-	PCIexpress Graphics Transmit - (10)	DP-O	-	-
D87	GND	Power Ground	PWR	-	-
D88	PEG_TX11+	PCIexpress Graphics Transmit + (11)	DP-O	-	-
D89	PEG_TX11-	PCIexpress Graphics Transmit - (11)	DP-O	-	-
D90	GND	Power Ground	PWR	-	-
D91	PEG_TX12+	PCIexpress Graphics Transmit + (12)	DP-O	-	-
D92	PEG_TX12-	PCIexpress Graphics Transmit - (12)	DP-O	-	-
D93	GND	Power Ground	PWR	-	-
D94	PEG_TX13+	PCIexpress Graphics Transmit + (13)	DP-O	-	-
D95	PEG_TX13-	PCIexpress Graphics Transmit - (13)	DP-O	-	-
D96	GND	Power Ground	PWR	-	-
D97	PEG_ENABLE#	PCIexpress Graphics Enable	I-3,3	PU 10k 3,3V	-
D98	PEG_TX14+	PCIexpress Graphics Transmit + (14)	DP-O	-	-
D99	PEG_TX14-	PCIexpress Graphics Transmit - (14)	DP-O	-	-
D100	GND	Power Ground	PWR	-	-
D101	PEG_TX15+	PCIexpress Graphics Transmit + (15)	DP-O	-	-
D102	PEG_TX15-	PCIexpress Graphics Transmit - (15)	DP-O	-	-
D103	GND	Power Ground	PWR	-	-
D104	VCC_12V	12V VCC	PWR	-	-
D105	VCC_12V	12V VCC	PWR	-	-
D106	VCC_12V	12V VCC	PWR	-	-
D107	VCC_12V	12V VCC	PWR	-	-
D108	VCC_12V	12V VCC	PWR	-	-
D109	VCC_12V	12V VCC	PWR	-	-
D110	GND	Power Ground	PWR	-	-

Note: The termination resistors in this table are already mounted on the ETXexpress® board. Refer to the design guide for information about additional termination resistors.

4.5 Alternative pinout of HDMI

Pin Nr.	Pin Name PCIexpress	Pin Name HDMI	HDMI Pin Description
D61	PCIexpress Graphics Transmit + 3	TMDS_B_CLK	HDMI Port B Clock
D62	PCIexpress Graphics Transmit - 3	TMDS_B_CLK#	HDMI port B Clock complement
D58	PCIexpress Graphics Transmit + 2	TMDS_B_DATA0	HDMI port B Data0
D59	PCIexpress Graphics Transmit - 2	TMDS_B_DATA0#	HDMI port B Data0 complement
D55	PCIexpress Graphics Transmit + 1	TMDS_B_DATA1	HDMI port B Data1
D56	PCIexpress Graphics Transmit - 1	TMDS_B_DATA1#	HDMI port B Data1 complement
D52	PCIexpress Graphics Transmit + 0	TMDS_B_DATA2	HDMI port B Data2
D53	PCIexpress Graphics Transmit - 0	TMDS_B_DATA2#	HDMI port B Data2 complement
C61	PCIexpress Graphics Receive + 3	TMDS_B_HPD#	HDMI port B Hot-plug detect
D74	PCIexpress Graphics Transmit + 7	TMDS_C_CLK	HDMI port C Clock
D75	PCIexpress Graphics Transmit – 7	TMDS_C_CLK#	HDMI port C Clock complement
D71	PCIexpress Graphics Transmit + 6	TMDS_C_DATA0	HDMI port C Data0
D72	PCIexpress Graphics Transmit – 6	TMDS_C_DATA0#	HDMI port C Data0 complement
D68	PCIexpress Graphics Transmit + 5	TMDS_C_DATA1	HDMI port C Data1
D69	PCIexpress Graphics Transmit – 5	TMDS_C_DATA1#	HDMI port C Data1 complement
D65	PCIexpress Graphics Transmit + 4	TMDS_C_DATA2	HDMI port C Data2
D66	PCIexpress Graphics Transmit – 4	TMDS_C_DATA2#	HDMI port C Data2 complement
C74	PCIexpress Graphics Receive + 7	TMDS_C_HDP#	HDMI port C Hot-plug detect

4.6 Alternative Pinout of Display Port

Pin Nr.	Pin Name PCIexpress	Pin Name HDMI	HDMI Pin Description
D61	PCIexpress Graphics Transmit + 3	DPB_LANE3	Displayport B Lane3
D62	PCIexpress Graphics Transmit – 3	DPB_LANE3#	Displayport B Lane3 complement
D58	PCIexpress Graphics Transmit + 2	DPB_LANE2	Displayport B Lane2
D59	PCIexpress Graphics Transmit – 2	DPB_LANE2#	Displayport B Lane2 complement
D55	PCIexpress Graphics Transmit + 1	DPB_LANE1	Displayport B Lane1
D56	PCIexpress Graphics Transmit - 1	DPB_LANE1#	Displayport B Lane1 complement
D52	PCIexpress Graphics Transmit + 0	DPB_LANE0	Displayport B Lane0
D53	PCIexpress Graphics Transmit – 0	DPB_LANE0#	Displayport B Lane0 complement
C61	PCIexpress Graphics Receive + 3	DPB_HPD#	Displayport B Hot-plug detect
C58	PCIexpress Graphics Receive + 2	DPB_AUX	Displayport B Aux
C59	PCIexpress Graphics Receive – 2	DPB_AUX#	Displayport B Aux complement
D74	PCIexpress Graphics Transmit + 7	DPC_LANE3	Displayport C Lane3
D75	PCIexpress Graphics Transmit – 7	DPC_LANE3#	Displayport C Lane3 complement
D71	PCIexpress Graphics Transmit + 6	DPC_LANE2	Displayport C Lane2
D72	PCIexpress Graphics Transmit – 6	DPC_LANE2#	Displayport C Lane2 complement
D68	PCIexpress Graphics Transmit + 5	DPC_LANE1	Displayport C Lane1
D69	PCIexpress Graphics Transmit – 5	DPC_LANE1#	Displayport C Lane1 complement
D65	PCIexpress Graphics Transmit + 4	DPC_LANE0	Displayport C Lane0
D66	PCIexpress Graphics Transmit – 4	DPC_LANE0#	Displayport C Lane0 complement
C74	PCIexpress Graphics Receive + 7	DPC_HPD#	Displayport C Hot-plug detect
C71	PCIexpress Graphics Receive + 6	DPC_AUX	Displayport C Aux
C72	PCIexpress Graphics Receive – 6	DPC_AUX#	Displayport C Aus complement

D88	PCIexpress Graphics Transmit + 11	DPD_LANE3	Displayport D Lane3
D89	PCIexpress Graphics Transmit – 11	DPD_LANE3#	Displayport D Lane3 complement
D85	PCIexpress Graphics Transmit + 10	DPD_LANE2	Displayport D Lane2
D86	PCIexpress Graphics Transmit – 10	DPD_LANE2#	Displayport D Lane2 complement
D81	PCIexpress Graphics Transmit + 9	DPD_LANE1	Displayport D Lane1
D82	PCIexpress Graphics Transmit – 9	DPD_LANE1#	Displayport D Lane1 complement
D78	PCIexpress Graphics Transmit + 8	DPD_LANE0	Displayport D Lane0
D77	PCIexpress Graphics Transmit – 8	DPD_LANE0#	Displayport D Lane0 complement
C88	PCIexpress Graphics Receive + 11	DPD_HPD#	Displayport D Hot-plug detect
C85	PCIexpress Graphics Receive + 10	DPD_AUX	Displayport D Aux
C86	PCIexpress Graphics Receive – 10	DPD_AUX#	Displayport D Aus complement

4.7 Signal Description

4.7.1 PCIexpress x1 lanes

The PCI express x1 lanes is a fast connection interface for many different system devices, such as network controllers, I/O controllers or express card devices. The implementation of this subsystem complies with the ETXexpress® / COMexpress Specification. Implementation information is provided in the ETXexpress® Design Guide. Refer to the documentation for additional information.

4.7.2 USB

Eight USB ports (EHCI high-speed 2.0 controller) are on the Intel® ICH-9M south bridge device available. The USB controllers comply with both versions 1.1 and 2.0 of the USB standard and are backward compatible.

Configuration

The USB controllers are PCI bus devices. The BIOS allocates required system resources during configuration of the PCI bus.

4.7.3 SATA

The Intel® ICH-9M south bridge device offers the possibility to connect 4 SATA Harddisks according SATA with 150 MB/s per channel or SATA II with 300 MB/s per channel in AHCI mode.

Configuration

The SATA controller is a PCI bus device. The BIOS allocates required system resources during configuration of the PCI bus.

4.7.4 Audio

The ETXexpress®-PC PCI HD audio controller is integrated in the Intel® ICH-9 Southbridge.

Configuration

The audio controller is a PCI bus device. The BIOS allocates required system resources during configuration of the PCI device.

4.7.5 Serial IRQ

The serial IRQ pin offers a standardized interface to link interrupt request lines to a single wire.

Configuration

The serial IRQ machine is in “Continuous Mode”

4.7.6 VGA Output

The ETXexpress®-PC graphics subsystem is integrated in the Intel® GS45 northbridge.

Configuration

The graphics controller requires the following resources:

- An IRQ
- Several I/O addresses
- Memory-address blocks in high memory

The BIOS allocates the resources during AGP configuration. Many resources are set for compatibility with industry-standard settings.

4.7.7 LVDS Flat Panel Interface (JILI)

The user interface for flat panels is the JUMPtec Intelligent LVDS Interface (JILI). The implementation of this subsystem complies with the ETXexpress® Specification. Implementation information is provided in the ETXexpress® Design Guide. Refer to the documentation for additional information.

4.7.8 PCIexpress Graphics

The PCI express Graphics interface allows the connection of high performace graphics chips on an high bandwidth interface.

The implementation of this subsystem complies with the ETXexpress® / COMexpress Specification. Implementation information is provided in the ETXexpress® Design Guide. Refer to the documentation for additional information.

4.7.9 SDVO

The ETXexpress®-CD Serial Digital Video Output port is integrated in the Intel® GS45 northbridge. It has the following features:

- Share its pins with the PEG interface

- Serial Digital Video Out Port (DVOB & DVOC) support
- Two 12-bit channels
- The SDVO B/C ports can drive a variety of SDVO devices (TV-Out Encoders, TMDS and LVDS transmitters, etc.)

The implementation of this subsystem complies with the ETXexpress® / COMexpress Specification. Implementation information is provided in the ETXexpress® Design Guide. Refer to the documentation for additional information.

4.7.10 HDMI

There is one HDMI port available shared together with PCIexpress Graphics, SDVO and Displayport.

4.7.11 Displayport

The display port is available shared together with PCIexpress Graphics, SDVO and HDMI.

4.7.12 Ethernet

The Ethernet interface offers 10 Mbit, 100Mbit or 1Gbit connection and is driven by the Intel® 82567 PCIexpress Gbit Ethernet controller.

Configuration

The Ethernet controller is a PCIexpress bus device. The BIOS allocates required system resources during configuration of the PCIexpress device.

4.7.13 Power Control

Power Good / Reset Input

The ETXexpress®-PC provides an external input for a power-good signal or a manual- reset pushbutton. The implementation of this subsystem complies with the ETXexpress® Specification. Implementation information is provided in the ETXexpress® Design Guide. Refer to the documentation for additional information.

4.7.14 Power Management

ATX PS Control

The ETXexpress®-PC can control the main power output of an ATX-style power supply. The implementation of this subsystem complies with the ETXexpress® Specification. Implementation information is provided in the ETXexpress® Design Guide. Refer to the documentation for additional information.

External SMI Interrupt

Contact Kontron Embedded Modules technical support for information on this feature.

4.7.15 Miscellaneous Circuits

Speaker

The implementation of the speaker output complies with the ETXexpress® Specification. Implementation information is provided in the ETXexpress® Design Guide. Refer to the documentation for additional information.

Battery

The implementation of the battery input complies with the ETXexpress® Specification. Implementation information is provided in the ETXexpress® Design Guide. Refer to the documentation for additional information.

In compliance with EN60950, there are at least two current-limiting devices (resistor and diode) between the battery and the consuming component.

I2C Bus

The I2C Bus is implemented by using GPIOs from the southbridge.

You also can access the I2C Bus via JUMPtec's Intelligent Device Architecture (JIDA) BIOS functions.

For additional information, refer to the ETXexpress® Design Guide, I2C application notes and JIDA specifications which are available at the Kontron Web site.

SM Bus

System Management (SM) bus signals are connected to the SM bus controller, which is located in the Intel® ICH-9M device. For more information about the SM bus, please see the System Management (SM) Bus section in the Appendix A: System Resources chapter.

LPC Bus

The Low Pin Count Interface signals are connected to the LPC Bus bridge, which is located in the Intel® ICH-9M. The LPC low speed interface can be used for peripheral circuits such as an external Super I/O Controller, which typically combine legacy-device support into a single IC. The implementation of this subsystem complies with the ETXexpress® Specification. Implementation information is provided in the ETXexpress® Design Guide. Refer to the documentation for additional information.

4.7.16 PCI Bus

The implementation of this subsystem complies with the ETXexpress® / COMexpress Specification. Implementation information is provided in the ETXexpress® Design Guide. Refer to the documentation for additional information.

4.7.17 IDE Port

The IDE host adapter is capable of DMA-33/66/100 operation. The implementation of this subsystem complies with the ETXexpress® Specification. Implementation information is provided in the ETXexpress® Design Guide. Refer to those documents for additional information.

Configuration

The IDE host adapter is a USB to IDE converter. It is configured by the BIOS during PCI device configuration. You can disable it in setup. Resources used by the USB/IDE host adapter are compatible with the PC/AT.

Warning: Current Operating Systems have problems or cannot be installed on an IDE device connected to an USB to IDE converter. Therefore the devices connected to this device must be seen as mass storage device and not as bootable or installable device

5 Special Features

5.1 Watchdog Timer

This feature is implemented in a watchdog PIC. You can configure the Watchdog Timer (WDT) in BIOS setup to start after a set amount of time after power-on boot. The WDT can also be controlled by the JIDA32 Library API (Refer to Appendix F: JIDA Standard). The application software should strobe the WDT to prevent its timeout. Upon timeout, the WDT resets and restarts the system. This provides a way to recover from program crashes or lockups.

Configuration

You can program the timeout period for the watchdog timer in two ranges:

- 1-second increments from 1 to 255 seconds
- 1-minute increments from 1 to 255 minutes

Contact Kontron Embedded Modules technical support for information on programming and operating the WDT.

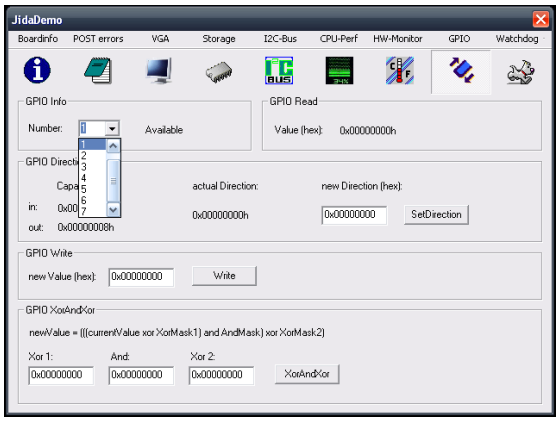
5.2 General Purpose Input and Output

ETXexpress®-PC offers 4 General Purpose Input (GPI) pins and 4 General Purpose Output (GPO) pins. On a 3.3V level digital in- and outputs are available.

Signal	Pin	Description
GPI0	A54	General Purpose Input 0
GPI1	A63	General Purpose Input 1
GPI2	A67	General Purpose Input 2
GPI3	A85	General Purpose Input 3
GPO0	A93	General Purpose Output 0
GPO1	B54	General Purpose Output 1
GPO2	B57	General Purpose Output 2
GPO3	B63	General Purpose Output 3

Configuration

The GPI and GPO pins can be configured via JIDA32. Please refer to the JIDA32 manual in the driver download packet on our website.

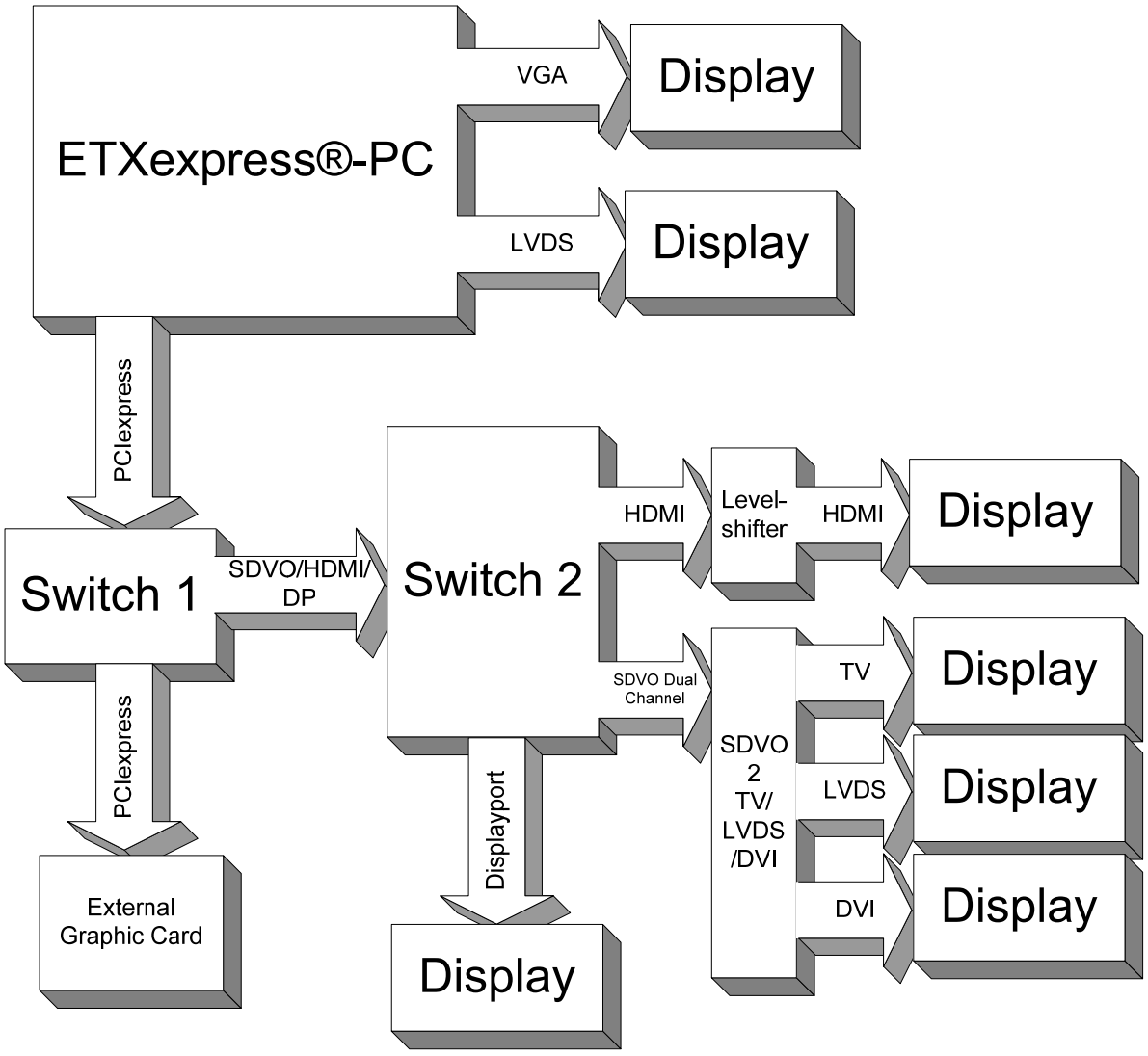


5.3 Usage of Different Graphic interfaces

5.3.1 Available Graphic interfaces

The ETXexpress®-PC offers VGA, PCIexpress, LVDS, HDMI, SDVO and Displayport interfaces to connect graphical user interfaces. The usage of VGA, PCIexpress and SDVO complies with the current ETXexpress® Specification.

The principle of using them is shown in the next drawing.



VGA and LVDS interface is always available and can be used. The pins of PCIexpress Graphics either are used as PCIexpress Graphics or as HDMI/SDVO/DP, which is controlled by switch1.

Switch1 is the SDVO_SDA# line (C73). When this signal is high (2.5V) the SDVO/HDMI/DP output is enabled. Otherwise the lines can be used as PCIexpressGraphic.

The switch 2 to select HDMI, SDVO or Displayport consists of the devices detected on the regarding sense circuits. When there is an SDVO 2 TV/LVDS/DVI converter found on the SDVO_DATA and _CLK lines (C73;

D73) then the output is switched to SDVO. When there is Displayport device found on the Displayport AUX lines (C71; C72) then it is Display port and in any other case the output is switched to HDMI.

6 Important Information

6.1 Cooling Solution

With introduction of higher frequency CPUs into the embedded market the need to design more efficient cooling solutions is now a necessity. These higher frequency CPUs generate much more heat, which must be removed from the application. One solution that has become more common in the embedded market is the use of heat pipes when designing a cooling solution. Kontron Embedded Modules has designed some cooling solutions that utilize heat pipes in order to perform some tests. Although Kontron Embedded Modules designed these cooling solutions strictly for test purposes, and not as a standard ETXexpress® cooling solution, the knowledge gained from these tests is being made available to customers in the form of an application note called PM_Thermal_Guidelines_E1xx.pdf. This application note should be used as a guideline to help evaluate potential thermal designs. It can be found on Kontron's web site at www.kontron.com on the ETXexpress® product page and in the Tech Support section.

6.2 Limitation

6.2.1 Reset Behavior

Intel® defined the Reset Behavior different to former Implementations. All former Boards and Modules had a level triggered reset input. ETXexpress-PC has according to the behavior change of the Intel® chipset an edge triggered reset input.

This leads to the fact that the board is not been able to keep in reset by holding down the signal.

6.2.2 Booting with a single memory module

When the board boots, the implemented Management Engine from Intel® needs the memory module be equipped in channel A, i.e. the module must be mounted in the bottom socket.

6.2.3 Standby with Microsoft Vista

Current (preliminary) revisions of the boards show none or not correct working standby (S3) behavior with Microsoft's Operating System Vista.

6.2.4 12V only

Current (preliminary) revisions of the boards don't work correctly in 12V only mode

6.2.5 IDE (PATA)

Current Operating Systems have problems or cannot be installed on an IDE device connected to an USB to IDE converter. Therefore the devices connected to this device must be seen as mass storage device and not as bootable or installable device.

There is only one IDE device working on the IDE port, no master slave capability.

6.2.6 Passive Cooling Trip Point

The BIOS setting for the Passive Cooling Trip Point doesn't work correctly in current (preliminary) revisions.

7 Design Considerations

7.1 Thermal Management

A heat-spreader plate assembly is available from Kontron Embedded Modules for the ETXexpress®-PC. The heat-spreader plate on top of this assembly is NOT a heat sink. It works as an ETXexpress®-standard thermal interface to use with a heat sink or other cooling device.

External cooling must be provided to maintain the heat-spreader plate at proper operating temperatures. Under worst-case conditions, the cooling mechanism must maintain an ambient air and heat-spreader plate temperature of 60° C or less.

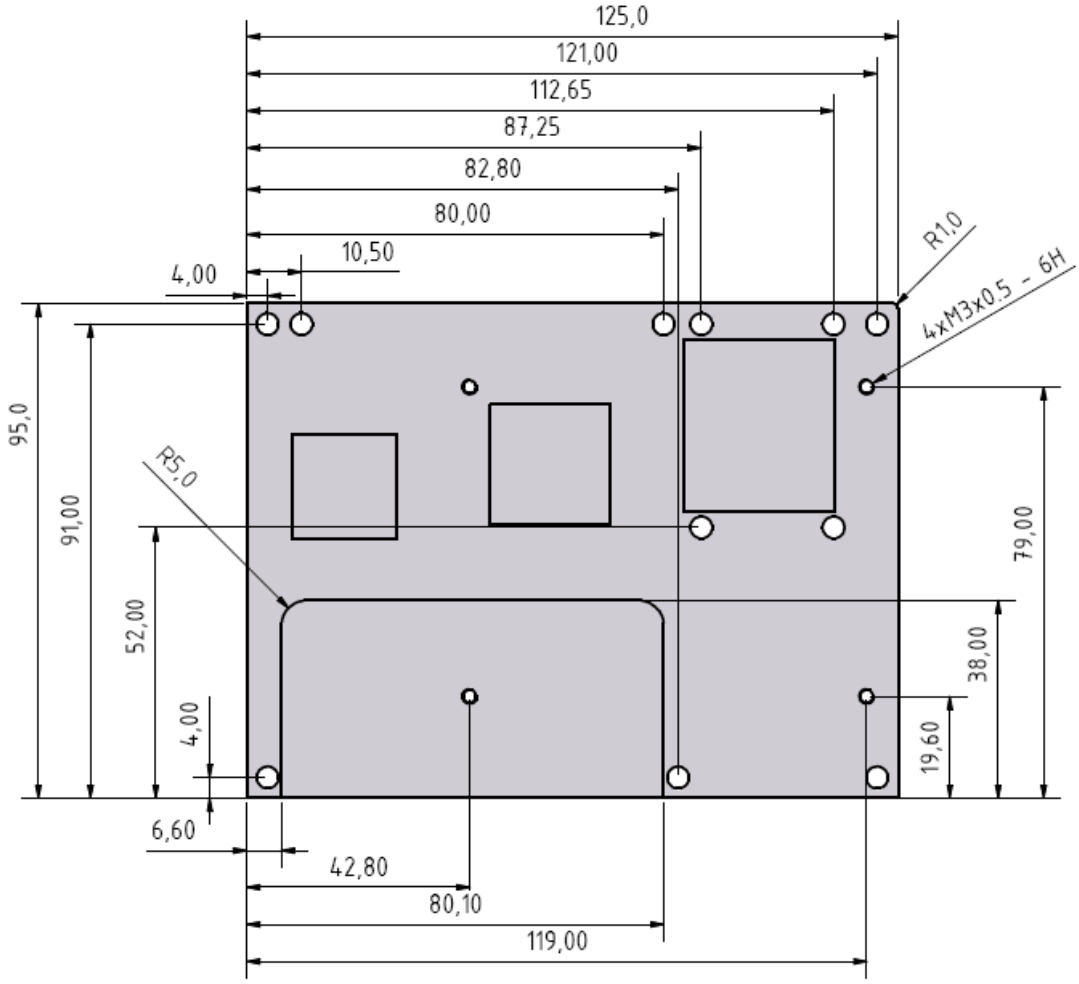
The aluminum slugs and thermal pads on the underside of the heat-spreader assembly implement thermal interfaces between the heat spreader plate and the major heat-generating components on the ETXexpress®-PC. About 80 percent of the power dissipated within the module is conducted to the heat-spreader plate and can be removed by the cooling solution.

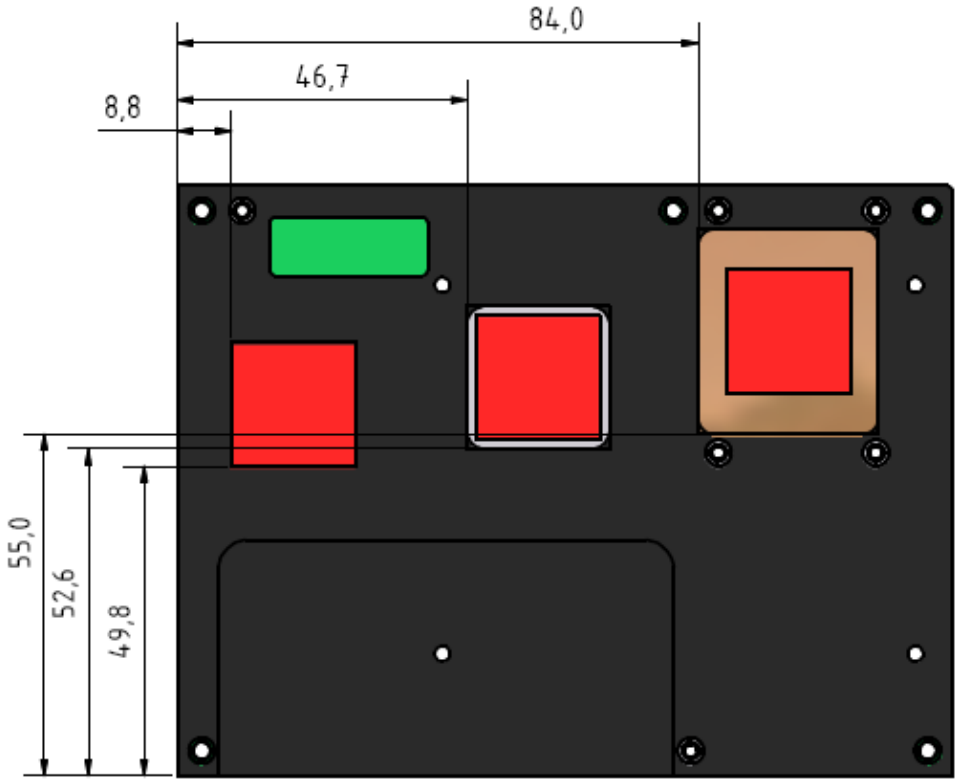
For 2266MHz modules, the heat dissipated into the plate ranges from 35 to 45 watts. Design a cooling solution to dissipate the heat load on a heat-spreader plate at a minimum of 45 watts to accommodate all ETXexpress®-PC modules.

You can use many thermal-management solutions with the heat-spreader plates, including active and passive approaches. The optimum cooling solution varies, depending on the ETXexpress® application and environmental conditions. Please see the ETXexpress® Design Guide for further information on thermal management.

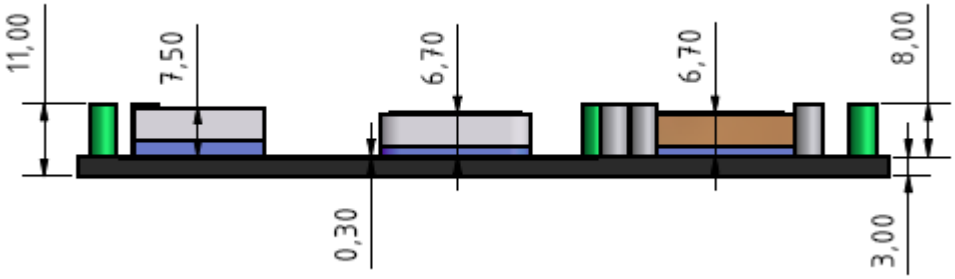
7.2 Heatspreader Dimensions

This is the backside view of the heatspreader plat with pads marked for the heat generating components for ETXexpress®-PC Modules.





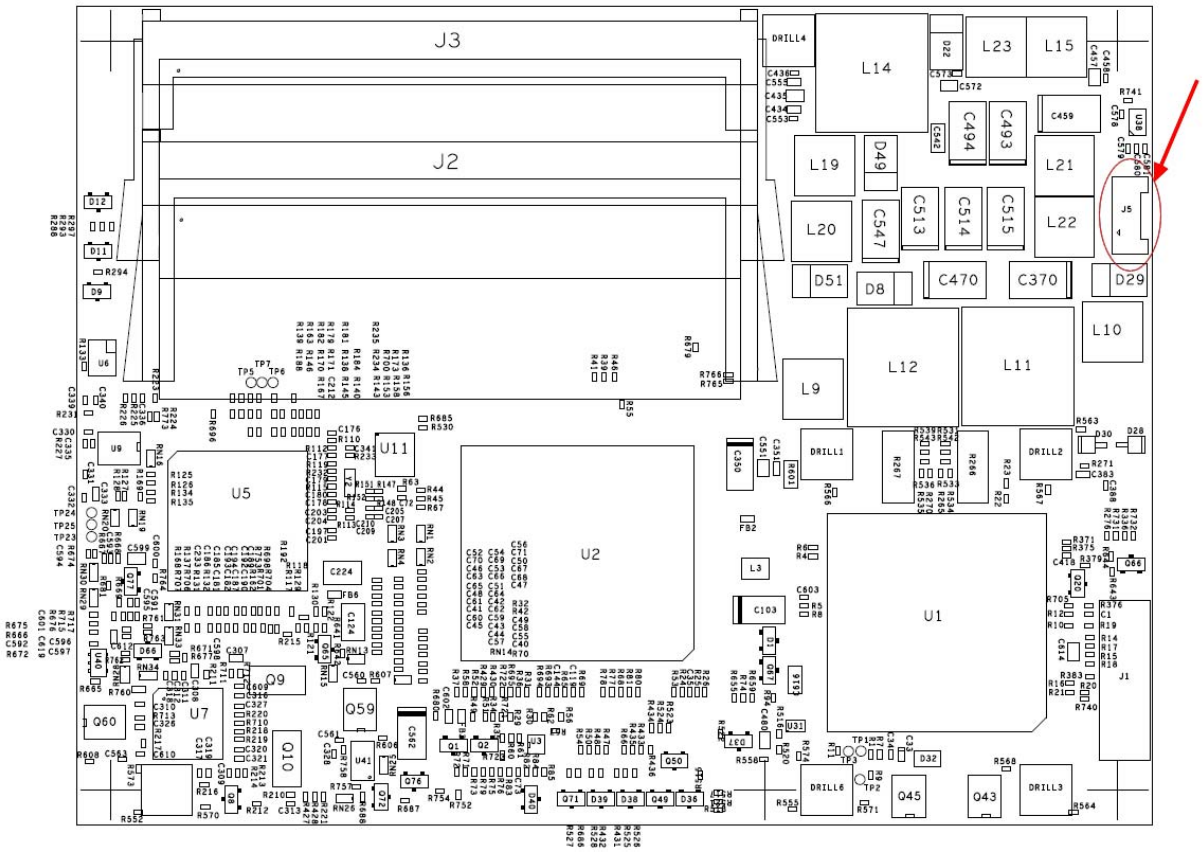
Sideview of the heat spreader:



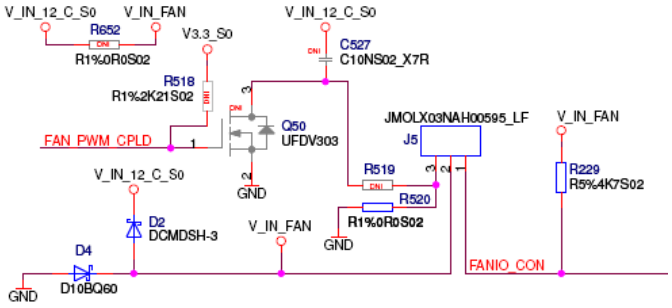
7.3 ETXexpress-PC onboard fan connector

This section describes how to connect a fan to the connector located directly on the ETXexpress®-PC. With certain BIOS-settings it is possible to control the fan depending on the Active Trip Point temperature. The fan switches on/off depending on the adjusted Active Trip Point temperature. In order for this feature to function properly an ACPI compliant OS is necessary.

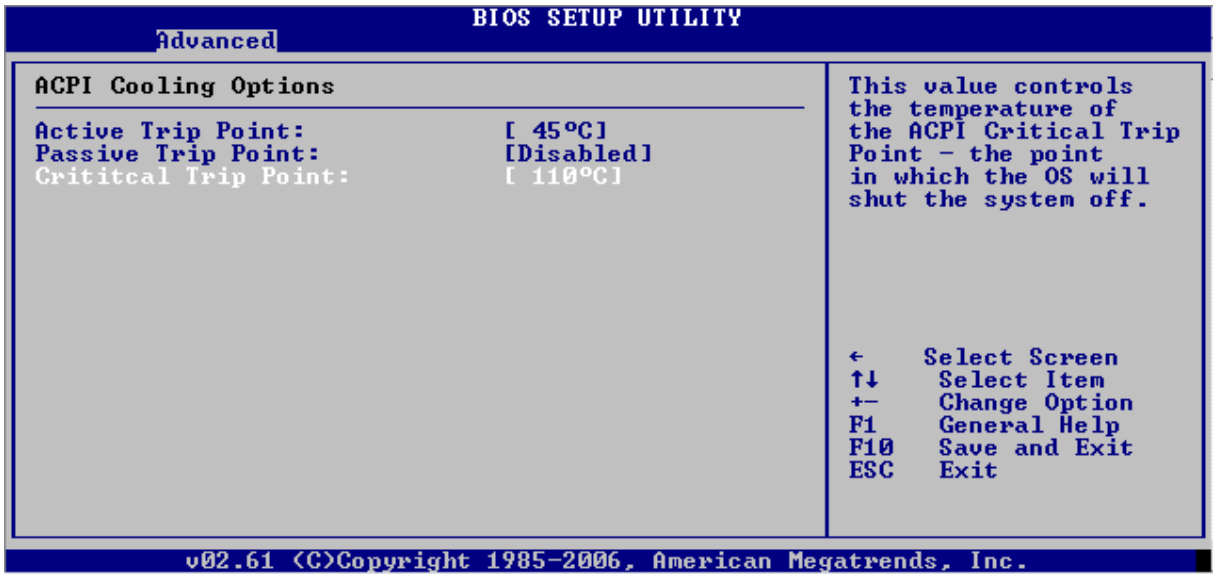
7.3.1 Location and pin-out of fan connector



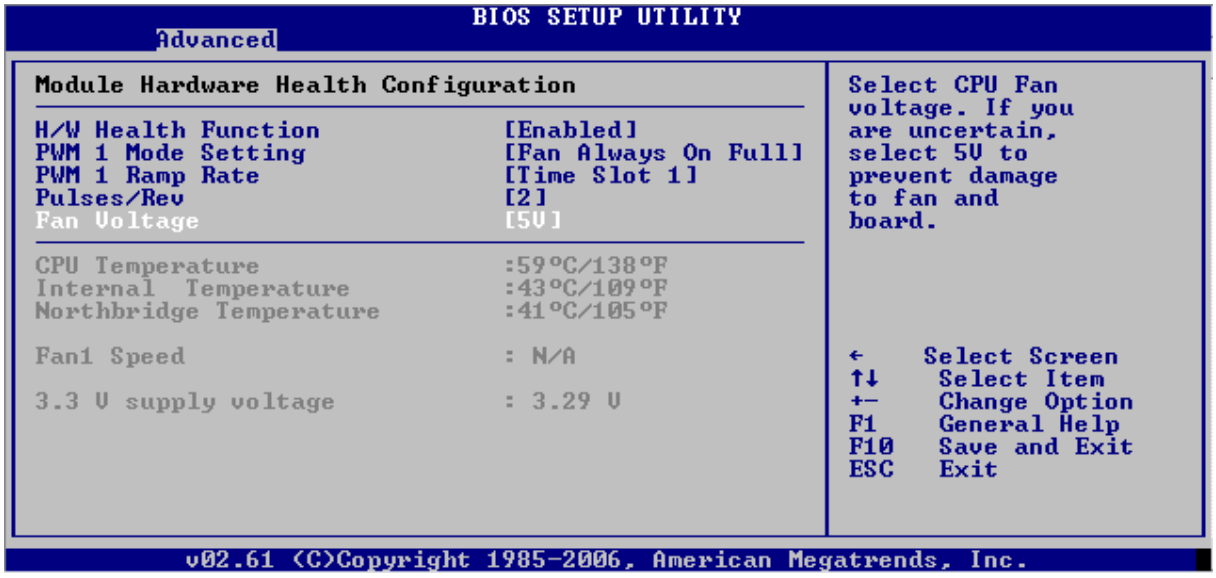
The onboard fan connector (J5) can be found at the right side opposite of the DRAM sockets and it is connected onboard according to the following schematic:



7.3.2 BIOS settings for fan control


BIOS SETUP UTILITY
Advanced
ACPI Cooling Options
Active Trip Point: [45°C]
Passive Trip Point: [Disabled]
Crititcal Trip Point: [110°C]
This value controls the temperature of the ACPI Critical Trip Point - the point in which the OS will shut the system off.
← Select Screen
↑↓ Select Item
+- Change Option
F1 General Help
F10 Save and Exit
ESC Exit
v02.61 (C)Copyright 1985-2006, American Megatrends, Inc.

The Active Trip Point controls the temperature when the fan is switched on and off.


BIOS SETUP UTILITY
Advanced
Module Hardware Health Configuration
H/W Health Function [Enabled]
PWM 1 Mode Setting [Fan Always On Full]
PWM 1 Ramp Rate [Time Slot 1]
Pulses/Rev [2]
Fan Voltage [5V]
CPU Temperature :59°C/138°F
Internal Temperature :43°C/109°F
Northbridge Temperature :41°C/105°F
Fan1 Speed : N/A
3.3 V supply voltage : 3.29 V
Select CPU Fan voltage. If you are uncertain, select 5V to prevent damage to fan and board.
← Select Screen
↑↓ Select Item
+- Change Option
F1 General Help
F10 Save and Exit
ESC Exit
v02.61 (C)Copyright 1985-2006, American Megatrends, Inc.

7.3.3 Electrical Characteristics

VCC_in_FANCON	=	VCC of board, limited to 12V
Imax	=	0,40 A

Note: The VCC_in_FANCON output is not short circuit proof. If necessary the user has to ensure that the circuit is protected externally, for example by a fuse on the backplane.

8 System Resources

8.1 Interrupt Request lines

Please be aware that an ACPI OS decides itself on resource usage. The tables below show only an example distribution.

In 8259 PIC mode

IRQ#	Used For	Available	Comment
0	Timer 0	No	
1	Keyboard	No	Note (4)
2	Slave 8259	No	
3		Yes	
4		Yes	
5		Yes	
6		Yes	
7		Yes	
8	RTC	No	
9	SCI	No	Note (3)
10		Yes	
11		Yes	
12	PS/2 Mouse	No	Note (5)
13	FPU	No	
14	IDE0	No	Note (1)(2)
15	IDE1	No	Note (1)(2)

Note: 1 If the "Used For" device is disabled in setup, the corresponding interrupt is available for other devices.
2 if sata controller is operating in legacy mode
3 Unavailable in Advanced Configuration and Power Interface (ACPI) mode. Used as System Control Interrupt (SCI) in ACPI mode. Currently not free in Non-ACPI mode.
4 used by legacy keyboard controller when available on carrier board.
5 used by legacy ps/2 mouse controller when available on carrier board.

In APIC mode

IRQ#	Used For	Available	Comment
0	Timer 0	No	
1	Keyboard	No	
2	Slave 8259	No	
3		Yes	Note (4)
4		Yes	Note (4)
5		Yes	Note (4)
6		Yes	Note (4)
7		Yes	Note (4)
8	RTC	No	
9	SCI	No	Note (2)
10		Yes	Note (4)
11		Yes	Note (4)
12		Yes	Note (4)
13	FPU	No	
14	IDE0	No	Note (1)(3)
15	IDE1	No	Note (1)(3)
16	PIRQ[A]	For PCI	PCI IRQ line 1 + Graphics controller + HD Audio Controller + secondary IDE Note (4)
17	PIRQ[B]	For PCI	PCI IRQ line 2 + HD Audio controller Note (4)
18	PIRQ[C]	For PCI	PCI IRQ line 3 + USB UCHI controller #3 + SATA (native mode) Note (4)
19	PIRQ[D]	For PCI	PCI IRQ line 4 + USB UCHI controller #2 + IDE (native mode) Note (4)
20	PIRQ[E]	No	Lan Controller Note (4)
21	PIRQ[F]	No	Note (4)
22	PIRQ[G]	No	Note (4)
23	PIRQ[H]	No	USB EHCI controller, USB UCHI controller #1 Note (4)

Note: 1 If the "Used For" device is disabled in setup, the corresponding interrupt is available for other devices.
2 Unavailable in Advanced Configuration and Power Interface (ACPI) mode. Used as System Control Interrupt (SCI) in ACPI mode. Currently not free in Non-ACPI mode.
3 IRQs are available if IDE controller is either disabled in setup or if in Native IDE mode.
4 ACPI OS decides on particular IRQ usage

8.2 Direct Memory Access (DMA) Channels

DMA#	Used For	Available	Comment
0		No	
1		No	
2		No	
3		No	
4	Cascade	No	
5		No	
6		No	
7		No	

8.3 Memory Area

Upper Memory	Used For	Available	Comment
C0000h-CFFFFh	VGA BIOS	No	
D0000h-DFFFFh		Yes	LPC Bus or Shadow RAM
E0000h-EFFFFh	System BIOS	No	

8.4 I/O Address Map

Upper Memory	Used For	Available	Comment
400h-41Fh	Chipset	No	Always used by chipset
4D0h-4D1h	Interrupt Controller	No	
500h-53Fh	Chipset	No	Always used by chipset
800h-87Fh	Chipset	No	Always used by chipset
1000h>	PCI	No	

8.5 Inter-IC (I2C) Bus

I2C Address	Used For	Available	Comment	JIDA Bus Nr.
A0h	JIDA-EEPROM	No	EEPROM for CMOS Data	0
A2h	JIDA-EEPROM	No		0

8.6 System Management (SM)Bus

I2C Address	Used For	Available	Comment	JIDA Bus Nr.
10h	SMB Hoste	No	EEPROM for CMOS Data	1
12h	SMART_Charger	No	Only be used by a SMB Charger	1
14h	SMART_Selector	No	Only be used by a SMB Selector	1
16h	SMART_Battery	No	Only be used by a SMB Battery	1
2Eh	HW-Monitor	No		1
A0h	SPD	No		1
A2h	SPD	No		1
D2h	Clockgenerator	No		1

8.7 JILI-I2C Bus

I2C Address	Used For	Available	Comment	JIDA Bus Nr.
A0h	JILI-EEPROM	No	EEPROM for CMOS Data	2

8.8 SDVO-I2C Bus

I2C Address	Used For	Available	Comment	JIDA Bus Nr.
A0h	DDC	No	Display Data	3

9 BIOS Operation

The module is equipped with AMI® BIOS, which is located in an onboard SPI serial flash memory. You can update the BIOS using a Flash utility.

9.1 Determining the BIOS Version

To determine the AMI® BIOS version, immediately press the Pause key on your keyboard as soon as you see the following text display in the upper left corner of your screen:

AMIBIOS © 2006 American Megatrends, Inc.

BIOS Date: 06/16/08 10:52:49 Ver: 08.00.14

Kontron® BIOS Version <CNTGRXXX>

© Copyright 2002-2008 Kontron Embedded Modules GmbH

9.2 Setup Guide

The AMIBIOS Setup Utility changes system behavior by modifying the BIOS configuration. The setup program uses a number of menus to make changes and turn features on or off.

Note: Selecting incorrect values may cause system boot failure. Load setup default values to recover by pressing <F9>.

9.2.1 Start AMI® BIOS Setup Utility

To start the AMI® BIOS setup utility, press <DEL> when the following string appears during bootup.

Press <DEL> to enter Setup

The Info Menu then appears.

The Setup Screen is composed of several sections:

Setup Screen	Location	Function
Menu Bar	Top	Lists and selects all top level menus.
Legend Bar	Right side Bottom	Lists setup navigation keys.
Item Specific Help Window	Right side Top	Help for selected item.
Menu Window	Left Center	Selection fields for current menu.
General Help Window	Overlay (center)	Help for selected menu.

Menu Bar

The menu bar at the top of the window lists different menus. Use the left/right arrow keys to make a selection.

Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The table below describes the legend keys and their alternates.

Key	Function
<F1> or <Alt-H>	General Help window.
<Esc>	Exit menu.
← or → Arrow key	Select a menu.
↑ or ↓ Arrow key	Select fields in current menu.
<Home> or <End>	Move cursor to top or bottom of current window.
<PgUp> or <PgDn>	Move cursor to next or previous page.
<F9>	Load the default configuration values for this menu.
<F10>	Save and exit.
<Enter>	Execute command or select submenu.
<Alt-R>	Refresh screen.

Selecting an Item

Use the ↑ or ↓ key to move the cursor to the field you want. Then use the + and – keys to select a value for that field. The Save Value commands in the Exit menu save the values displayed in all the menus.

Displaying Submenus

Use the ← or → key to move the cursor to the submenu you want. Then press <Enter>. A pointer (▸) marks all submenus.

Item Specific Help Window

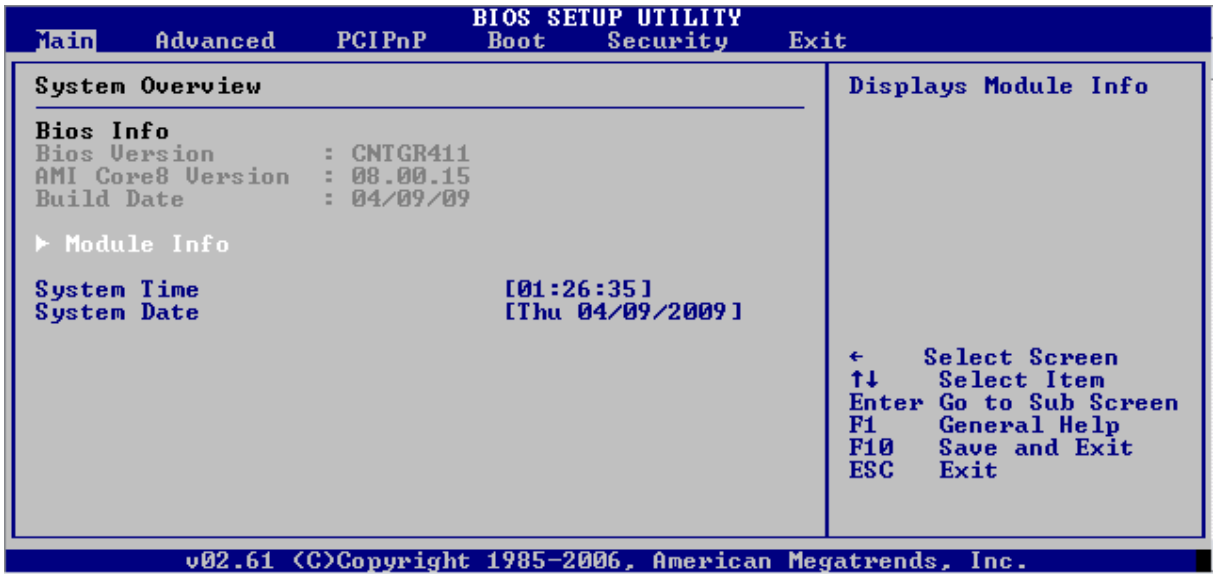
The Help window on the right side of each menu displays the Help text for the selected item. It updates as you move the cursor to each field.

General Help Window

Pressing <F1> or <Alt-F1> on a menu brings up the General Help window that describes the legend keys and their alternates. Press <Esc> to exit the General Help window.

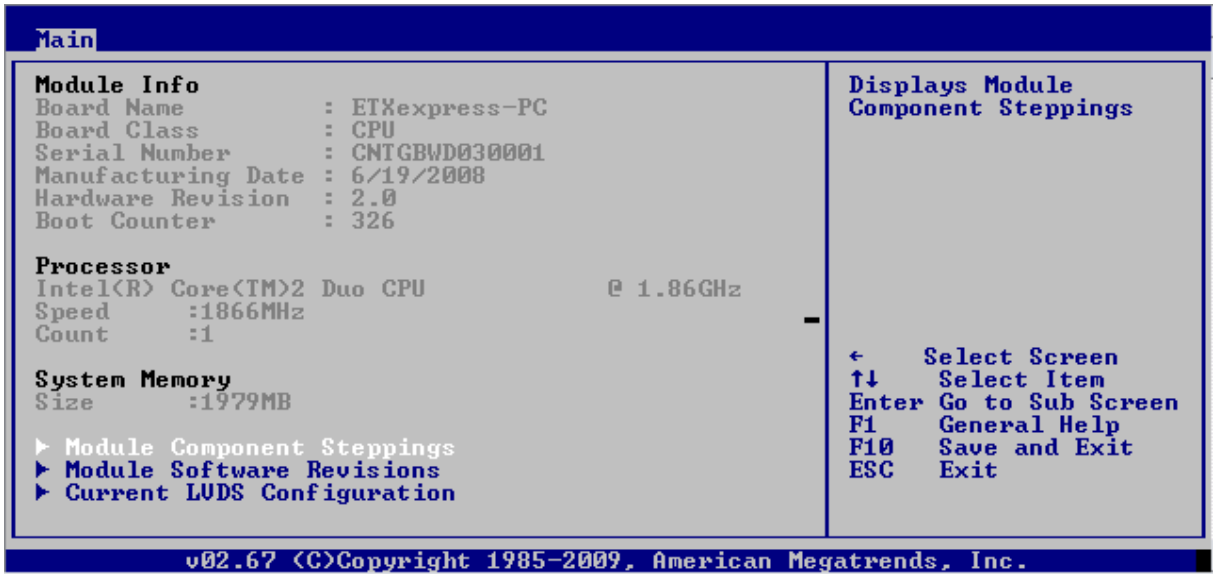
9.3 BIOS Setup Menus

9.3.1 Main Menu

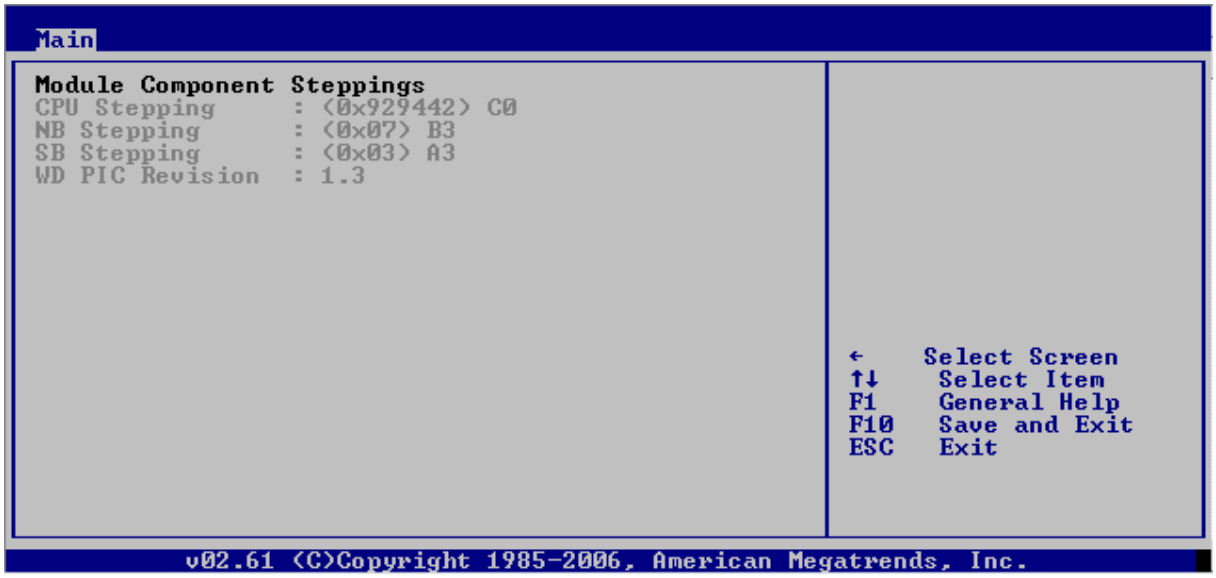


Feature	Option	Description
System Time	[hh:mm:ss]	<Tab>, <Shift-Tab>, or <Enter> selects field
System Date	[mm-dd-yyyy]	<Tab>, <Shift-Tab>, or <Enter> selects field

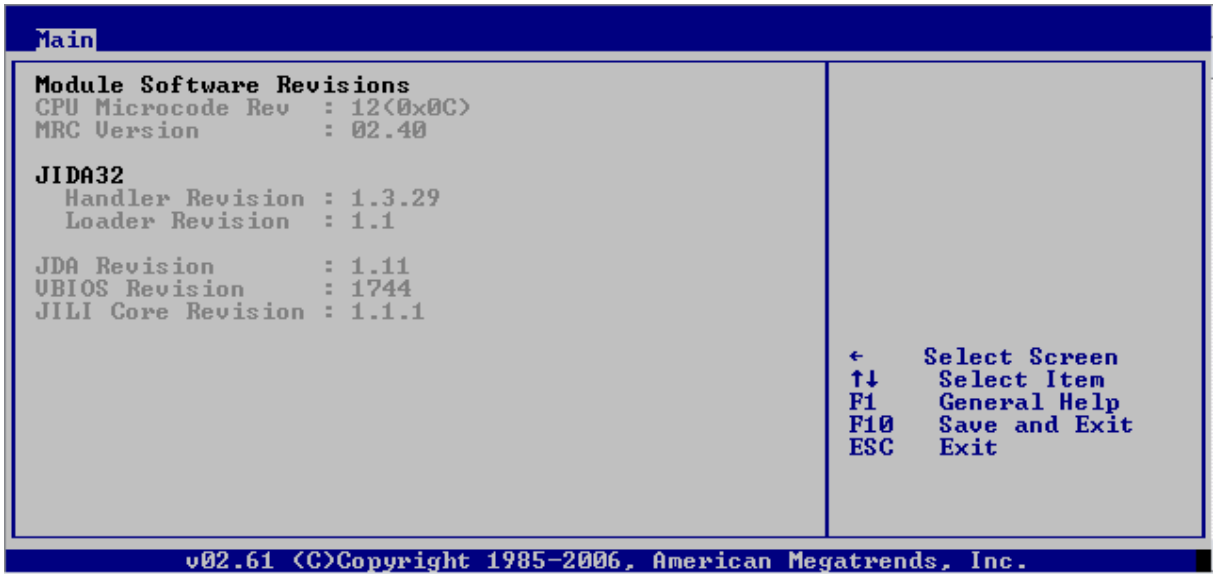
Module Info



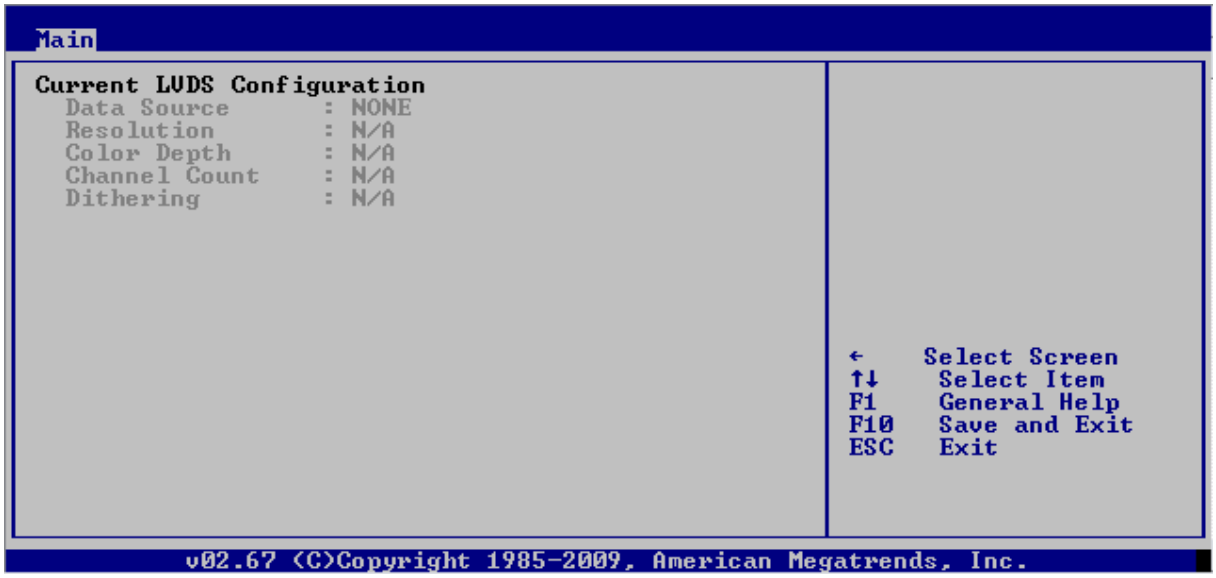
Module Component Steppings



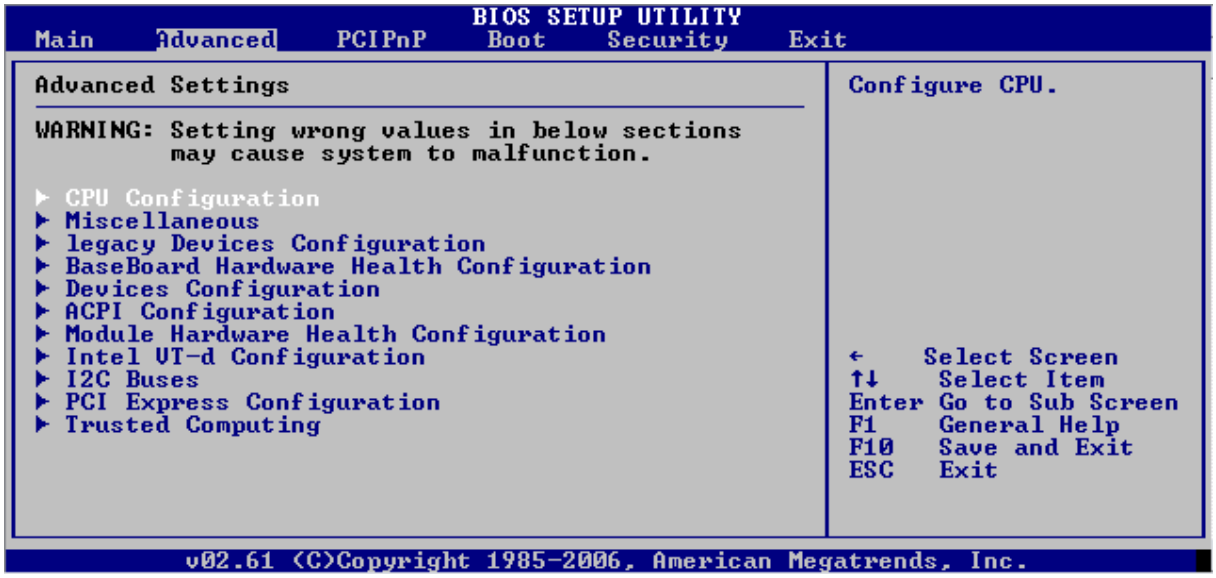
Module Software Revisions



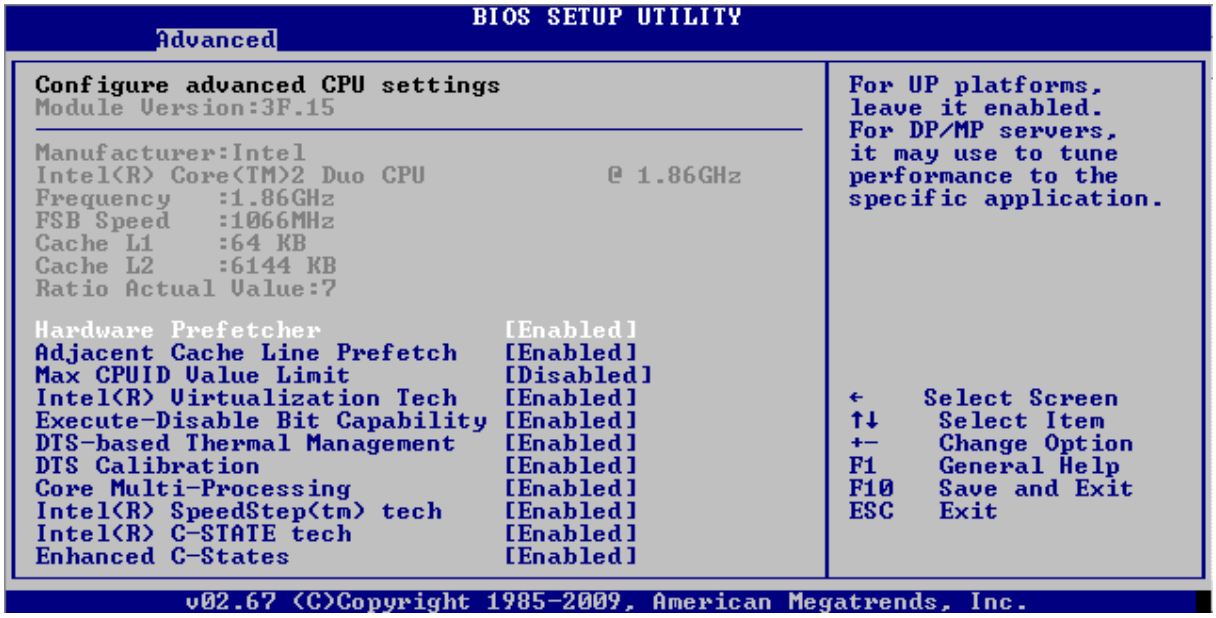
Current LVDS Configuration



9.3.2 Advanced Menu

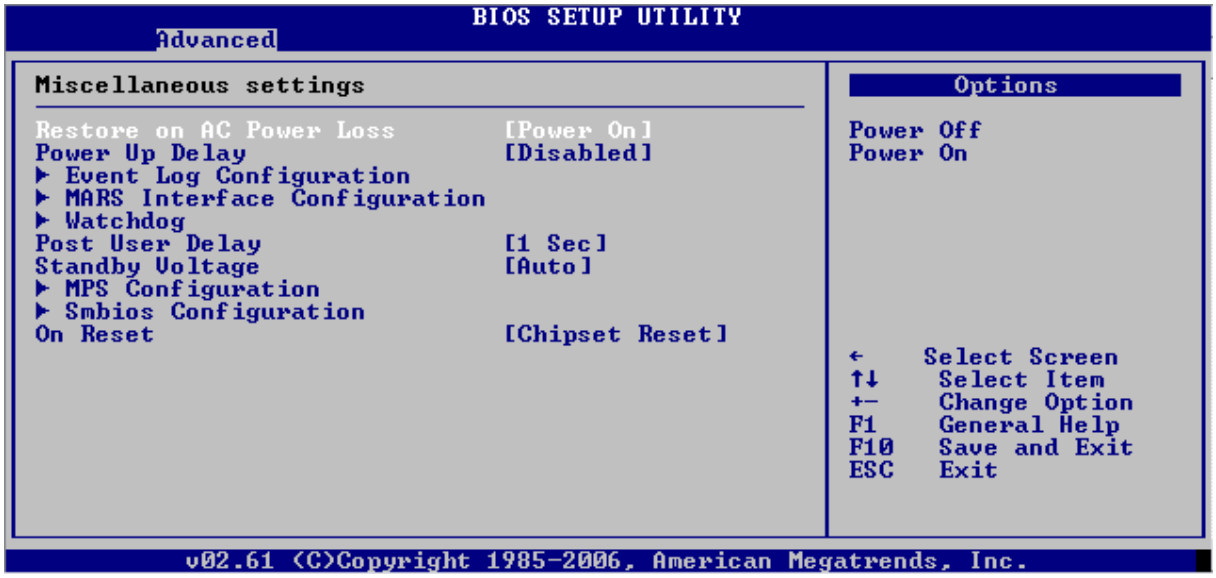


CPU Configuration



Feature	Option	Description
Hardware Prefetcher	**Enabled** Disabled	Disables and Enables the Hardware Prefetcher
Adjacent Cache Line Prefetch	**Enabled** Disabled	For UP platforms, leave it enabled
MAX CPUID Value Limit	Enabled **Disabled**	Enables the MAX CPUID Value Limit. Should be disabled for Windows XP
Execute-Disable Bit Capability	**Enabled** Disabled	Enables and Disables the Execute-Disable Bit Capability
DTS-based Thermal Management	**Enabled** Disabled	Enables and Disables the DTS-based Thermal Management
DTS Calibration	**Enabled** Disabled	Enables and Disables the DTS Calibration
Intel ® SpeedStep™ tech	**Enabled** Disabled	Enables and Disables the Speed Stepping Feature
Intel ® C-STATE tech	**Enabled** Disabled	Enables and Disables the C-STATE technology
Enhanced C-States	**Enabled** Disabled	Enables and Disables the Enhanced C - States

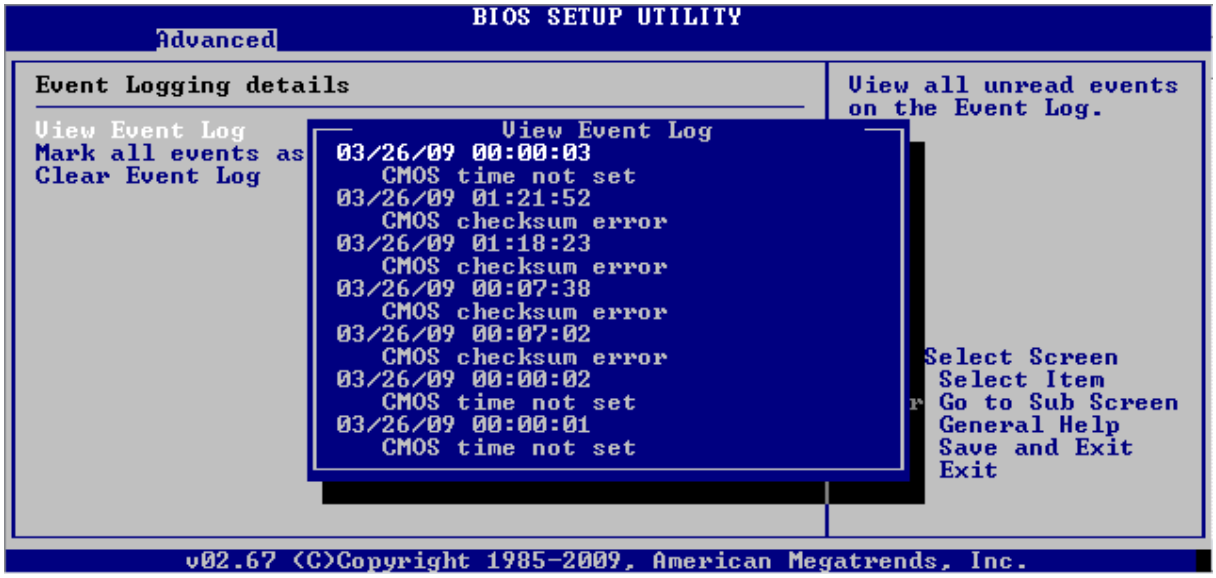
Miscellaneous Settings Menu



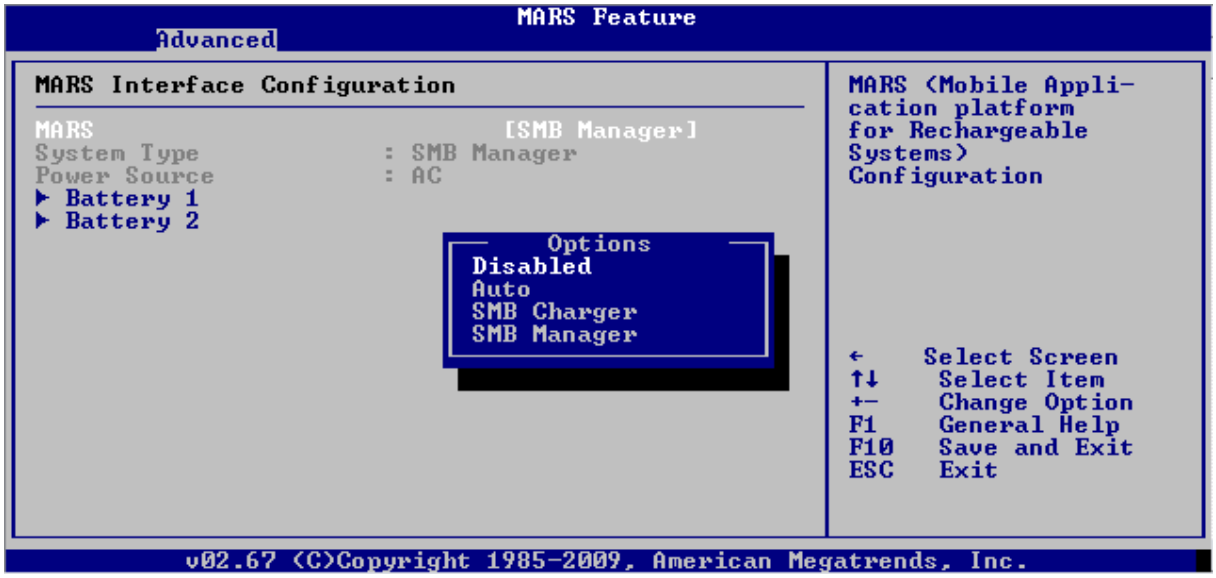
Feature	Option	Description
Restore on AC Power Loss	Power Off **Power On**	Selects the behavior of switch on process after AC Power Loss
Power Up Delay	**Disabled** 4 to 5 seconds 3 to 4 seconds 2 to 3 seconds 1 to 2 seconds	Select Delay for the Power Up
Post User Delay	None **1 Sec** 2 Sec ... 10 Min	Delay to allow access to setup
Standby Voltage	**Auto** 5V Standby	Select which voltage is used for standby power.
On Reset	**Chipset Reset** Power Cycle	Chipset Reset: only edge triggered reset Power Cycle: level triggered reset

Note: Intel® changed the specification of the chipset reset which is not corresponding to the COMexpress specification anymore. Chipset Reset confirms to the Intel® chipset behaviour and is level triggered only. The board can be held in a reset state. Power Cycle allows still level triggered usage, which complies with the COMexpress specification, but creates a complete power cycle of the board.

Event Log Configuration

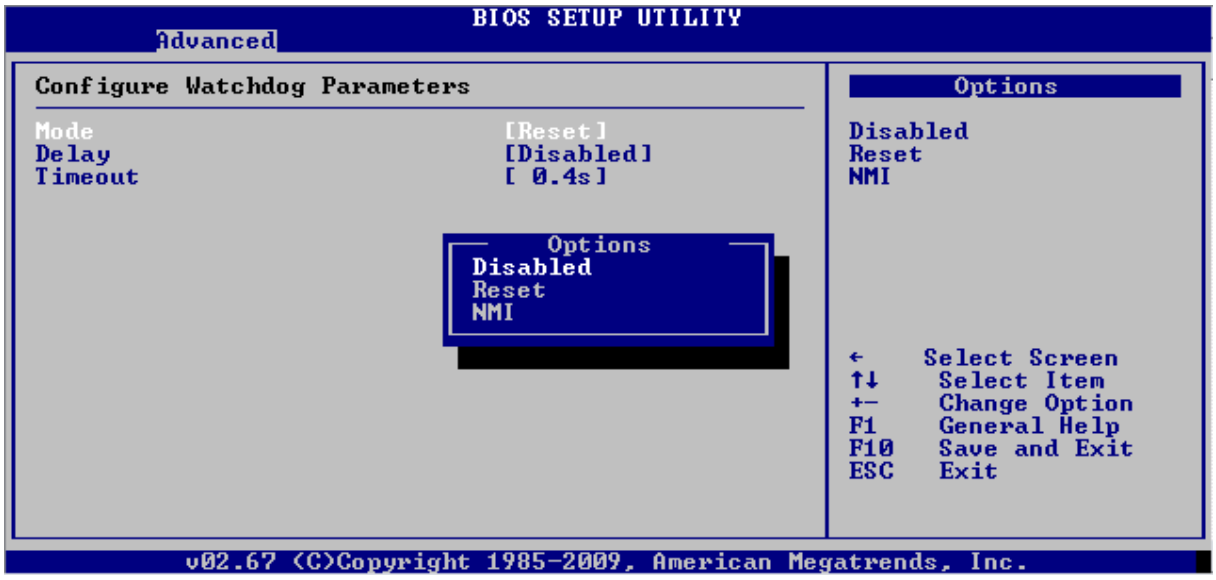


MARS Interface Configuration Menu



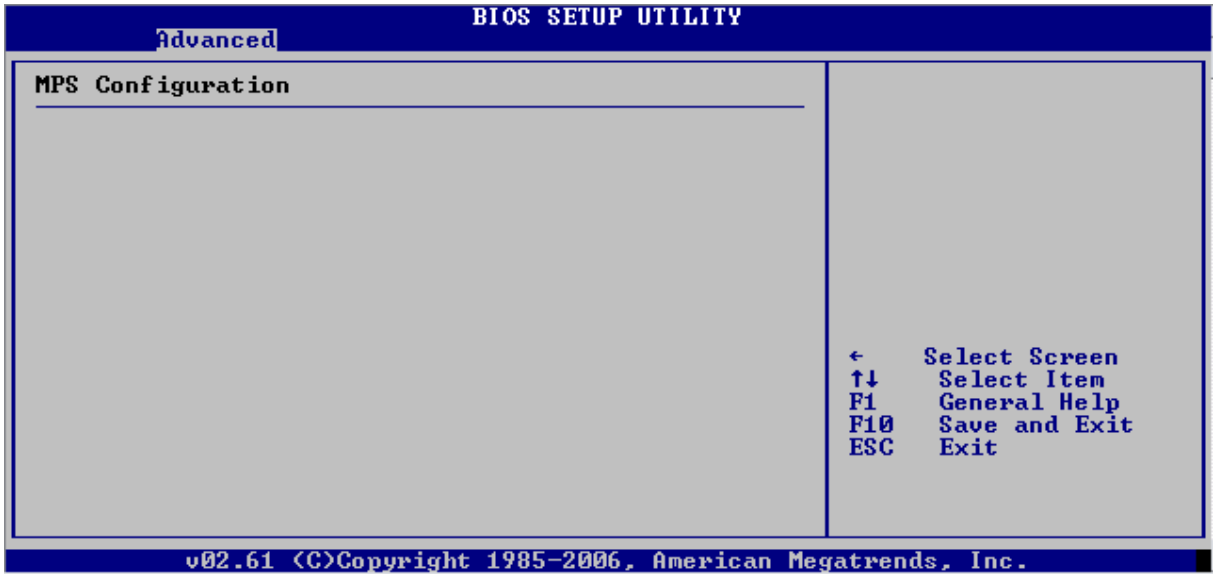
Feature	Option	Description
MARS	**Disabled** Auto SMB Charger SMB Manager	Selects how to handle the SMB Controller, either as SMB Charger for one battery or as SMB Manager for up to two batteries

Watchdog Menu



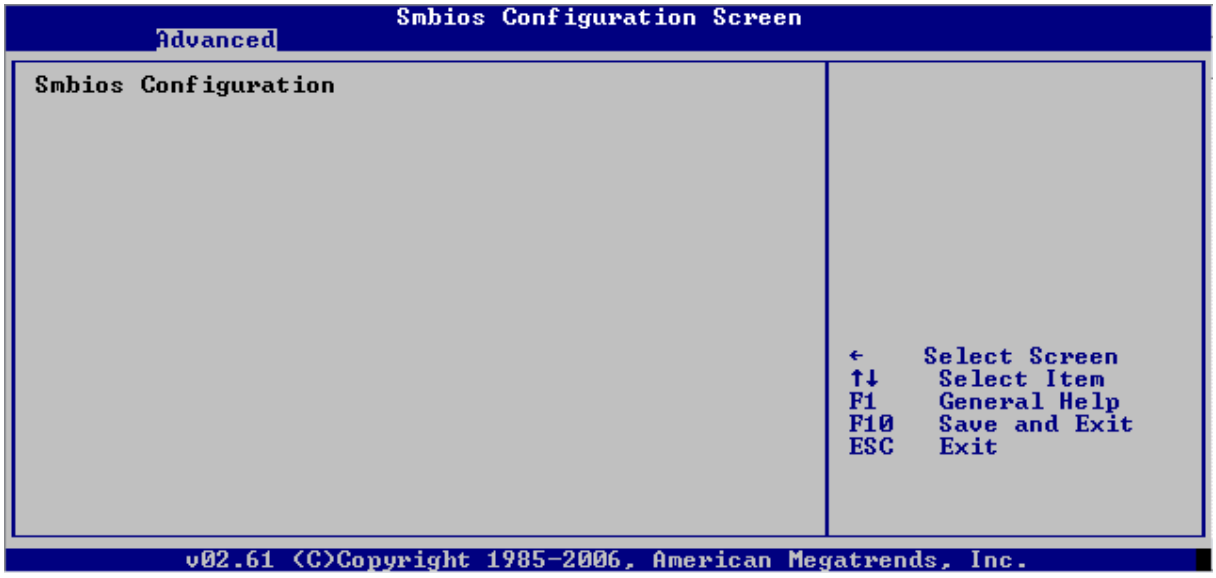
Feature	Option	Description
Mode	**Disabled** Reset NMI	Disables or selects the mode for the
Delay	**Disabled** 1s 5s 10s ... 30:00m	Set the Delay until the timer will start
Timeout	**0.4s** 1s 5s ... 10:00m	Set the timeout until the watchdog has to be triggered

MPS Configuration Menu



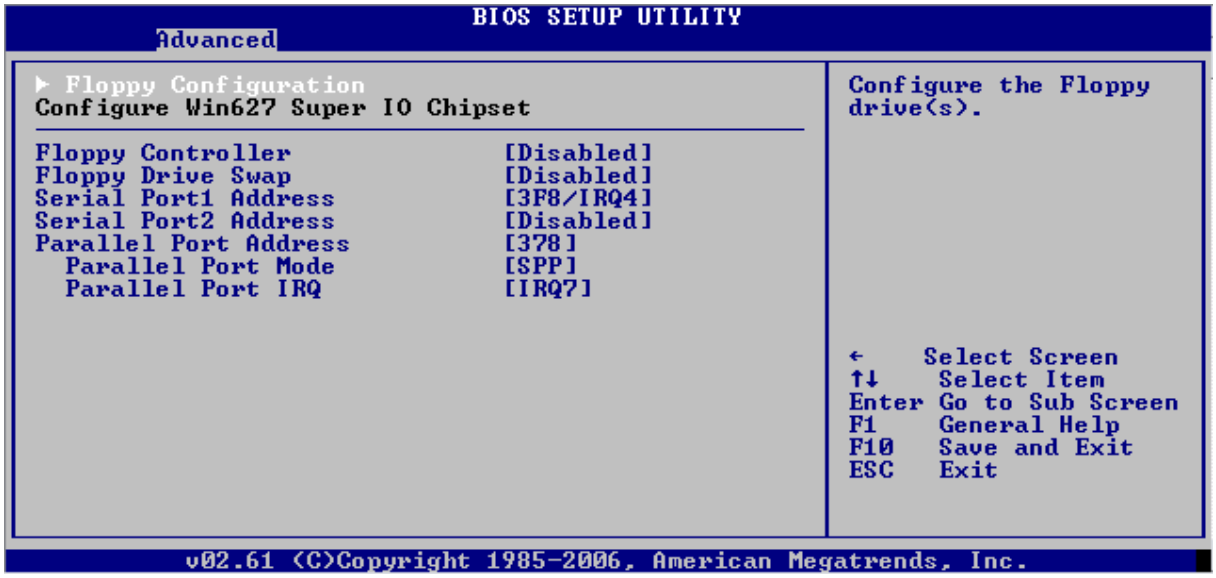
Note: Currently not supported

Smbios Configuration



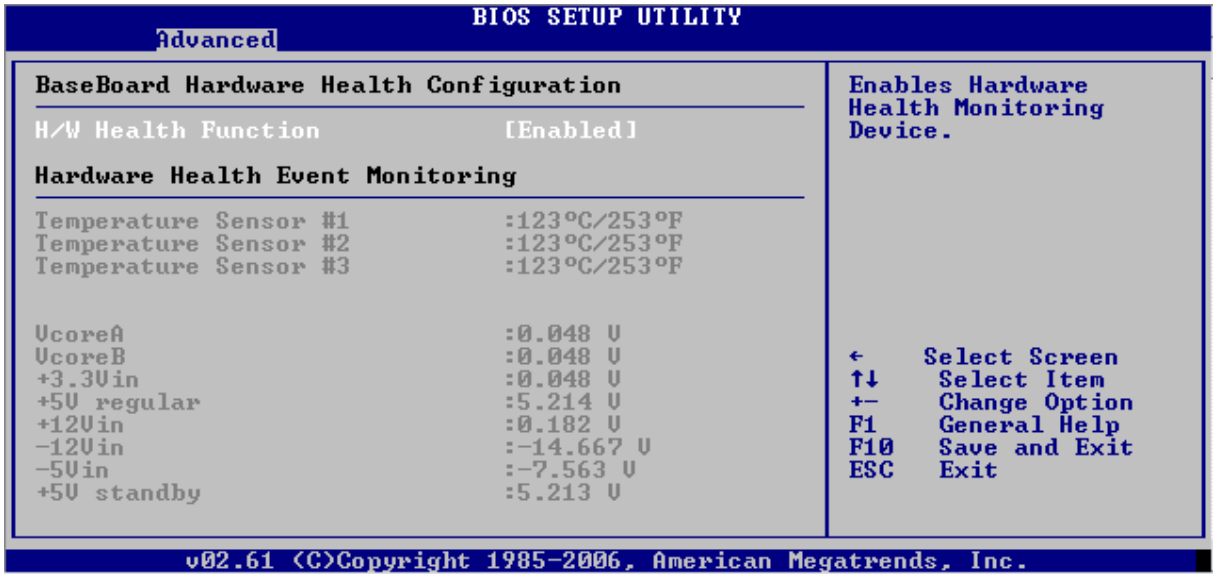
Note: Currently not supported

Legacy Device Configuration Menu



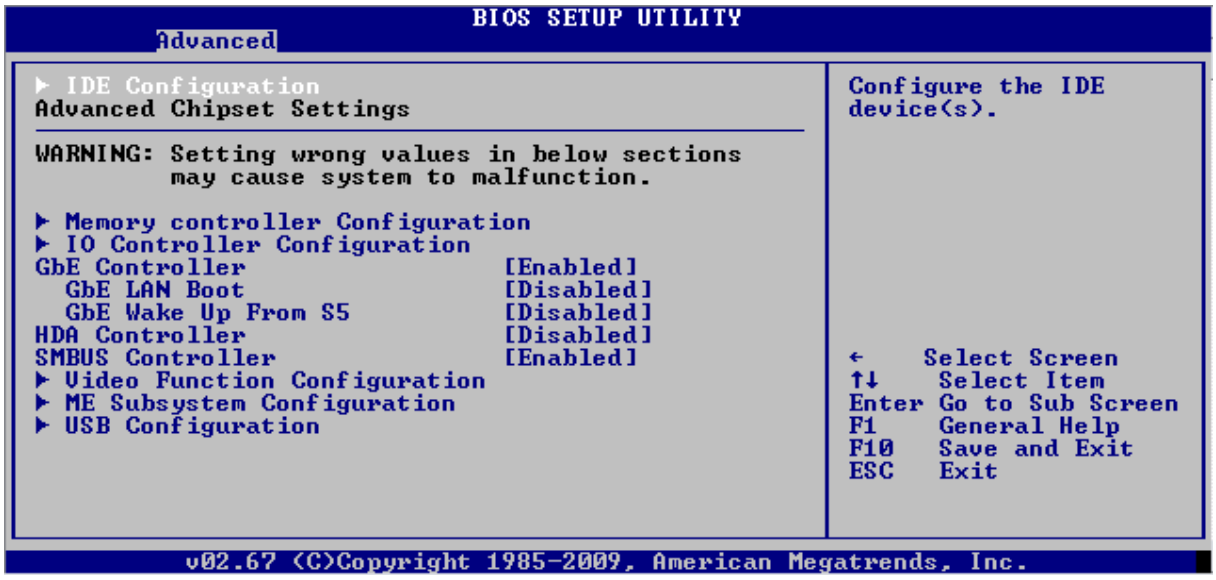
Feature	Option	Description
Onboard Floppy Controller	**Disabled** Enabled	Disables or Enables the floppy interface of the Winbond Super I/O controller (backplane)
Floppy Drive Swap	**Disabled** Enabled	Select if the 2 floppy devices are swapped
Serial Port1 Address	Disabled **3F8/IRQ4** 2F8/IRQ3 3E8/IRQ 4 2E8/IRQ3	Selects the Resources for COMA of the Winbond Super/O controller
Serial Port2 Address	**Disabled** 3F8/IRQ4 2F8/IRQ3 3E8/IRQ 4 2E8/IRQ3	Selects the Resources for COMB of the Winbond Super I/O controller
Parallel Port Address	Disabled **378** 278 3BC	Selects the Resources for LPT of the Winbond Super I/O controller
Parallel Port Mode	**SPP** Bi-Directional ECP EPP + SPP ECP + EPP	Selects the Mode for LPT of the Winbond Super I/O controller
Parallel Port IRQ	**IRQ7** IRQ5	Selects the Resources for LPT of the Winbond Super I/O controller

Baseboard Hardware Health Configuration



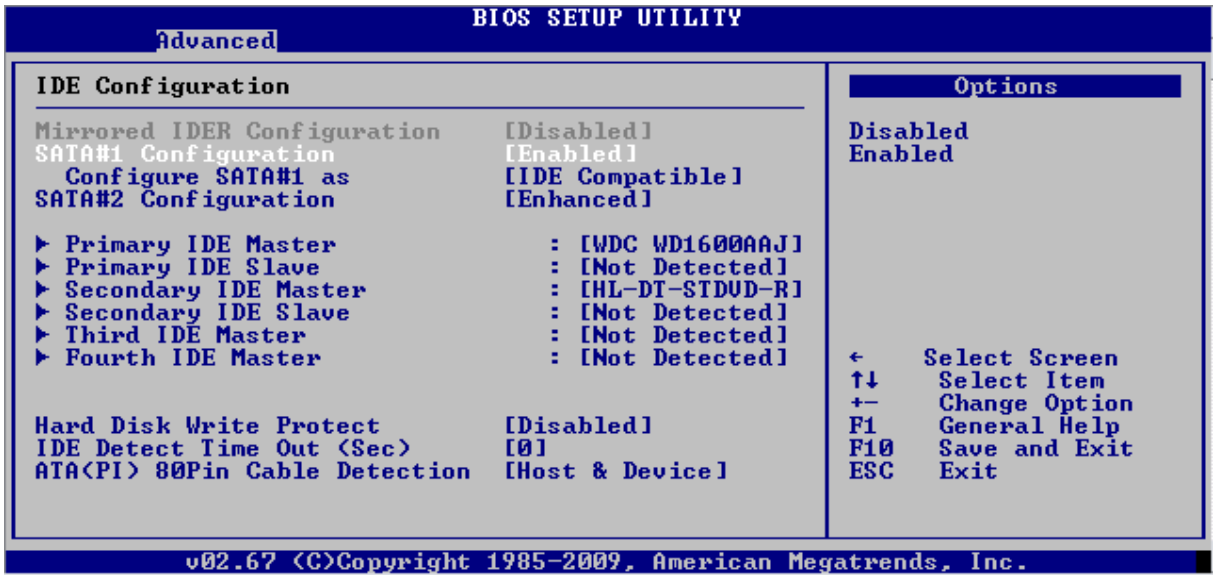
Feature	Option	Description
H/W Health Function	**Enabled** Disabled	Enables and disables the H/W monitor of the baseboard Winbond SuperI/O controller

Devices Configuration Menu



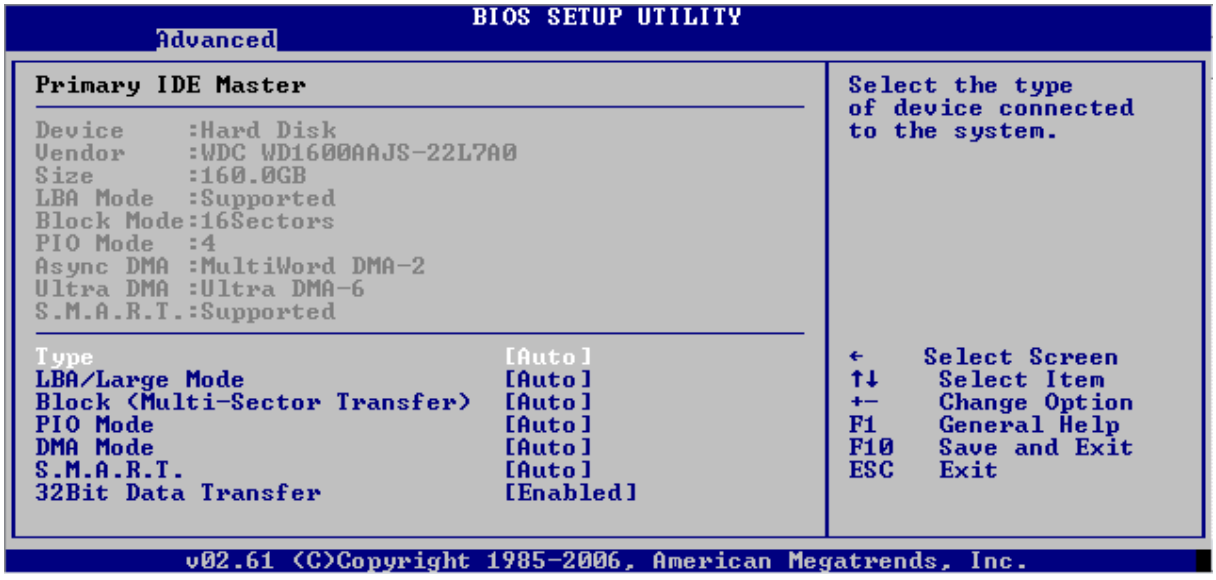
Feature	Option	Description
GbE Controller	**Enabled** Disabled	Configure the LAN Controller
GbE LAN Boot	**Disabled** Enabled	Configure the LAN boot feature (PXE)
GbE Wake Up From S5	**Disabled** Enabled	Configure if the board will wake up via WOL from S5
HDA Controller	**Disabled** Enabled	Disables and Enables the HDA audio controller
SMBUS Controller	**Enabled** Disabled	Disables and Enables the SMBUS Controller

IDE Configuration Menu



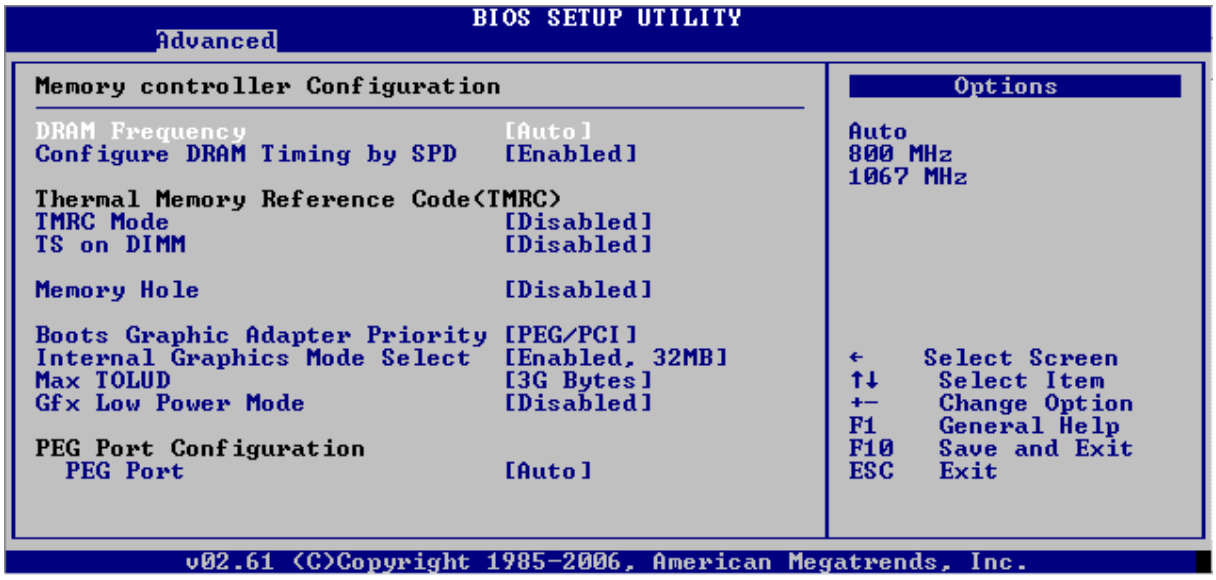
Feature	Option	Description
SATA#1 Configuration	**Enabled** Disabled	Enables and Disables the SATA interface functional block #1
Configure SATA #1 as	**IDE Compatible** RAID AHCI IDE Enhanced	Configure the SATA mode
SATA#2 Configuration	**Enhanced** Disabled	Configures the SATA interface functional block #2
Primary IDE Master Primary IDE Slave Secondary ... Fourth IDE Master	**Shows the detected Device**	Enters the device configuration page
Hard Disk Write Protect	**Disabled** Enabled	Enables and disables the hard disk write protect (only valid in BIOS/DOS mode)
IDE Detect Time Out (Sec)	0 5 .. 30 **35**	Selects the time out for IDE device detection in seconds
ATA(PI) 80Pin Cable Detection	**Host&Device** Host Device	Selects the mechanism for detecting 80pin ATA(PI) cable

IDE Device Configuration Menu



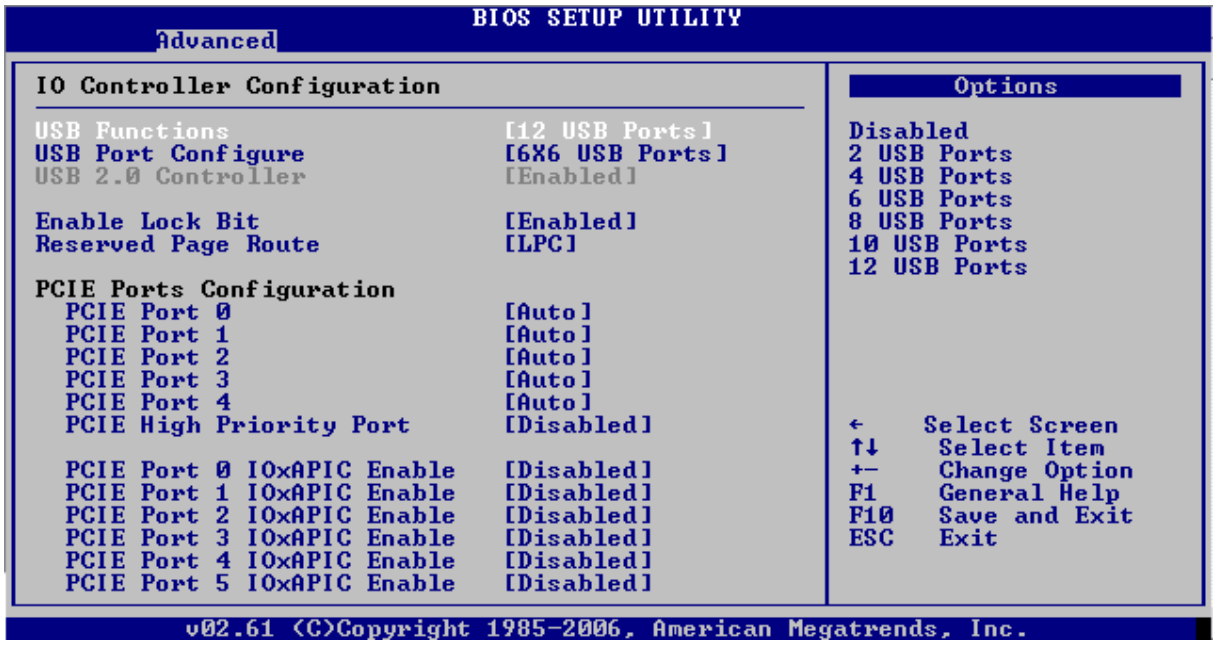
Feature	Option	Description
Type	No Installed **Auto** CD/DVD ARMD	Selects the type of device connected to the system
LBA/Large Mode	**Auto** Disabled	Autodetects or disables the LBA Mode
Block (Multi-Sector Transfer)	**Auto** Disabled	Autodetects or disables the Block Mode
PIO Mode	**Auto** 0 ... 4	Autodetects or selects the PIO mode
DMA Mode	**Disabled** Enabled	Enables and disables the hard disk write protect (only valid in BIOS/DOS mode)
S.M.A.R.T.	**Auto** Disabled Enabled	Autodetects, enables or disables the Self-Monitoring, Analysis and Reporting Tool
32Bit Data Transfer	**Host&Device** Host Device	Selects the mechanism for detecting 80pin ATA(PI) cable

Memory Controller Configuration Menu



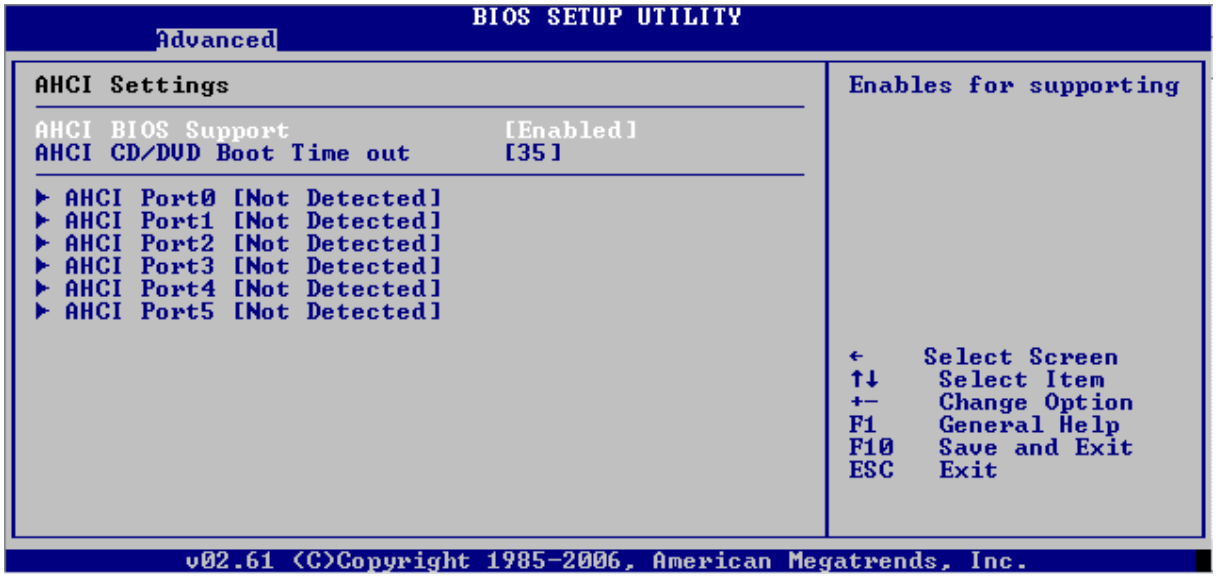
Feature	Option	Description
DRAM Frequency	**Auto** 800 MHz 1067 MHz	Selects the DRAM Frequency
Configure DRAM Timing by SPD	**Enabled** Disabled	Selects if DRAM is configured by SPD-EEPROM
TMRC Mode	**Disabled** Enabled	Enables and Disables the Thermal Memory Reference Code Feature
TS on DIMM	**Disabled** Enabled	Enables and Disables thermal sensor on DIMM
Memory Hole	**Disabled** 15-16MB	Enables and Disables the extended memory hole
Boot Graphic Adapter Priority	IGD PCI/IGD PCI/PEG PEG/IGD **PEG/PCI**	Selects which graphiccontroller to use as primary boot device: IGD: internal graphic controller PEG: PCI express graphics PCI: PCI graphic card
Internal Graphics Mode Select	Disabled **Enabled, 32 MB** Enabled, 64 MB Enabled, 128 MB	Selects the amount of system memory used by the internal graphics device
Max TOLUD	**3G Bytes** 2.5G Bytes 2G Bytes	Selects the maximum of Top of low usable DRAM
Gfx Low Power Mode	**Disabled** Enabled	Enables and disables the low power mode for the graphics device
PEG Port	**Auto** Disabled Enabled	Enables, disables or auto configures the PCIexpress graphics port

I/O Controller Configuration Menu



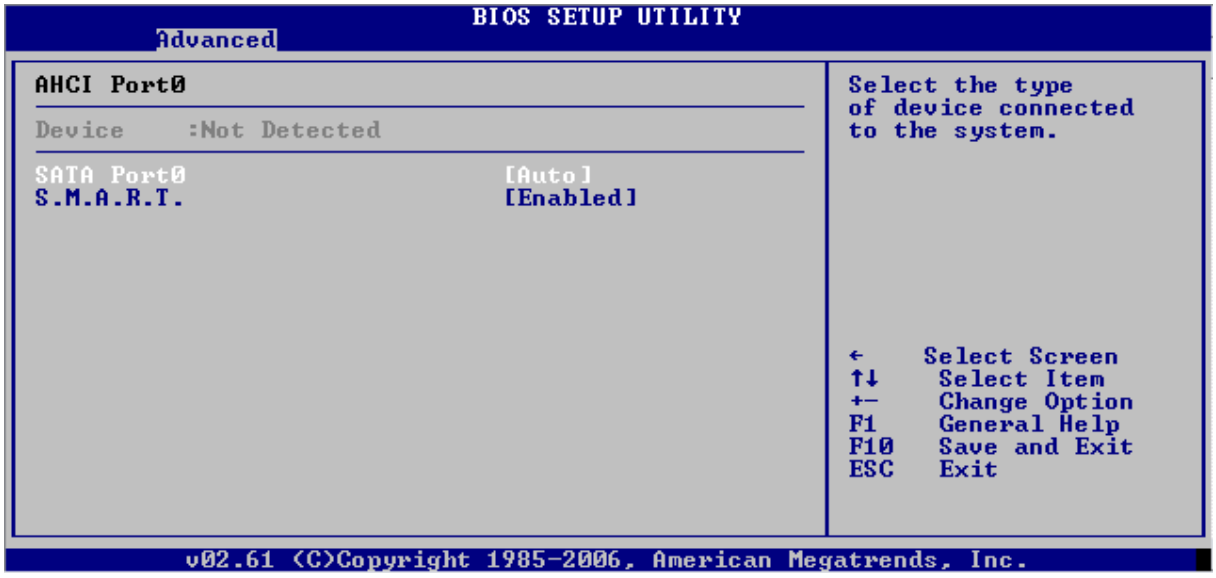
Feature	Option	Description
USB Function	Disabled 2 USB Ports 4 USB Ports ... 10 USB Ports **12 USB Ports**	Selects the amount of enabled USB ports
USB Port Configure	**6x6 USB Ports** 4x8 USB Ports	Configures the chipset internal USB port configuration
USB 2.0 Controller	Disabled **Enabled**	Enables and Disables USB 2.0 Controller
Enable Lock Bit	Disabled **Enabled**	Enables Lock bit at end of POST. Only disable for debugging purposes.
Reserve Page Route	**LPC** PCI	Selects the Inteface for Port 80h output during POST
PCIE Ports 0...4	**Auto** Enabled Disabled	Selects the mode for the PCIexpress ports
PCIE High Priority Port	**Disabled** Port 0 Port 1 ... Port 5	Selects which PCIe Port has higher priority than the others
PCIE Port 0...5 IOxAPIC Enable	**Disabled** Enabled	Enables and Disables the IOxAPIC function for PCIe ports

AHCI Settings Menu



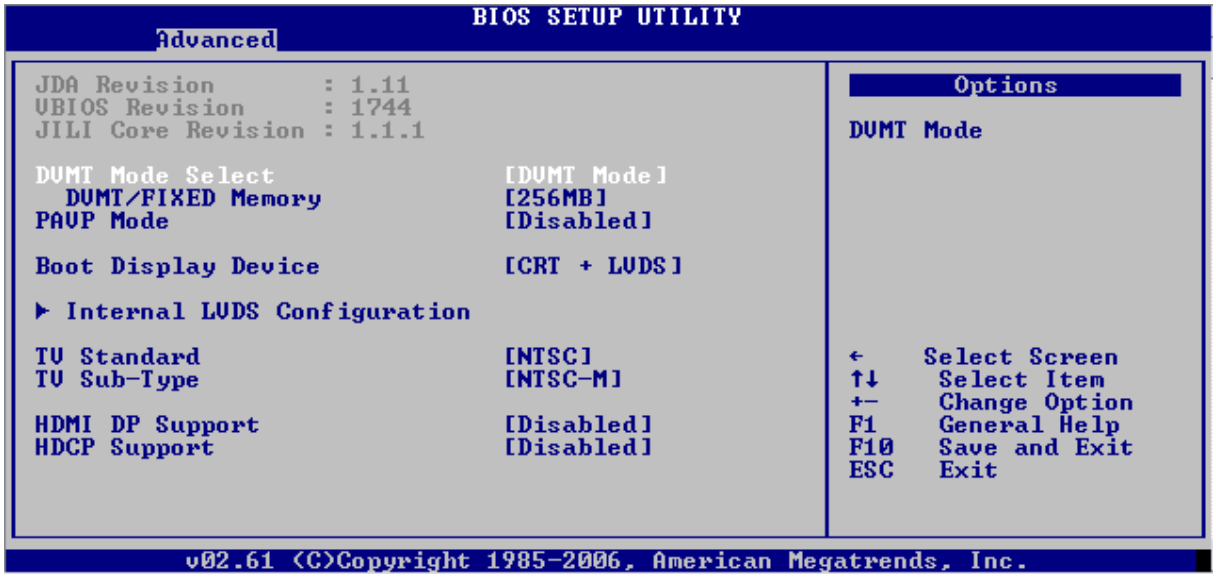
Feature	Option	Description
AHCI BIOS Support	**Enabled** Disabled	Enables or Disables the AHCI feature for SATA
AHCI CD/DVD Boot Time out	0 5 ... 30 **35**	Set the Boot Time out of the SATA CD/DVD devices in AHCI mode

AHCI Portx Menu



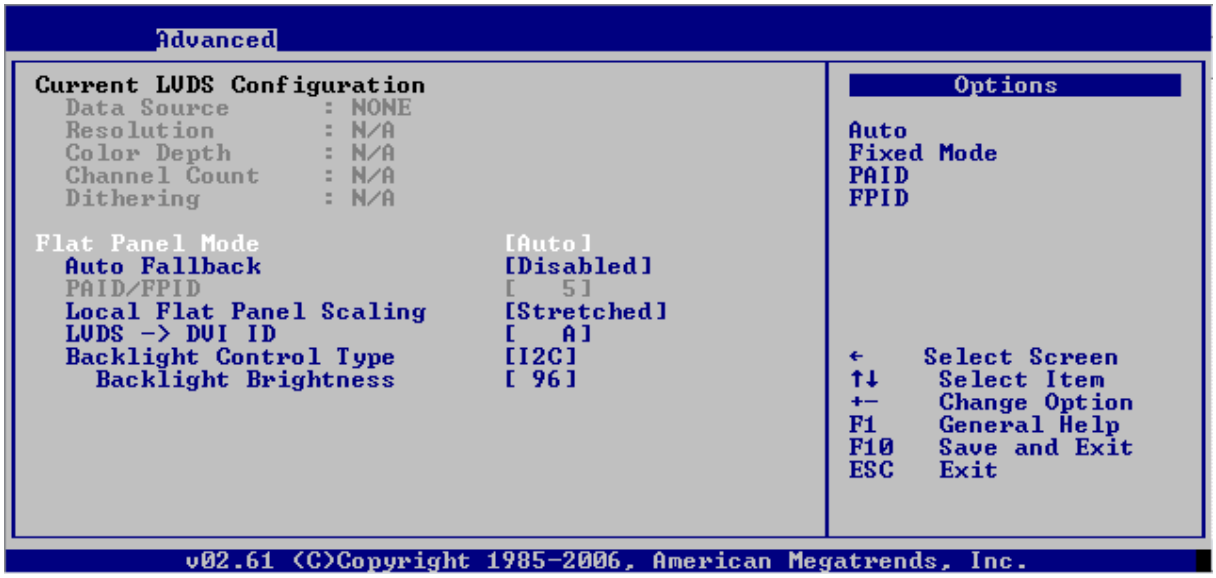
Feature	Option	Description
SATA Portx	**Auto** Not Installed	Configures the individual SATA port
S.M.A.R.T.	**Enabled** Disabled	Enables or disables the Self-Monitoring, Analysis and Reporting Tool

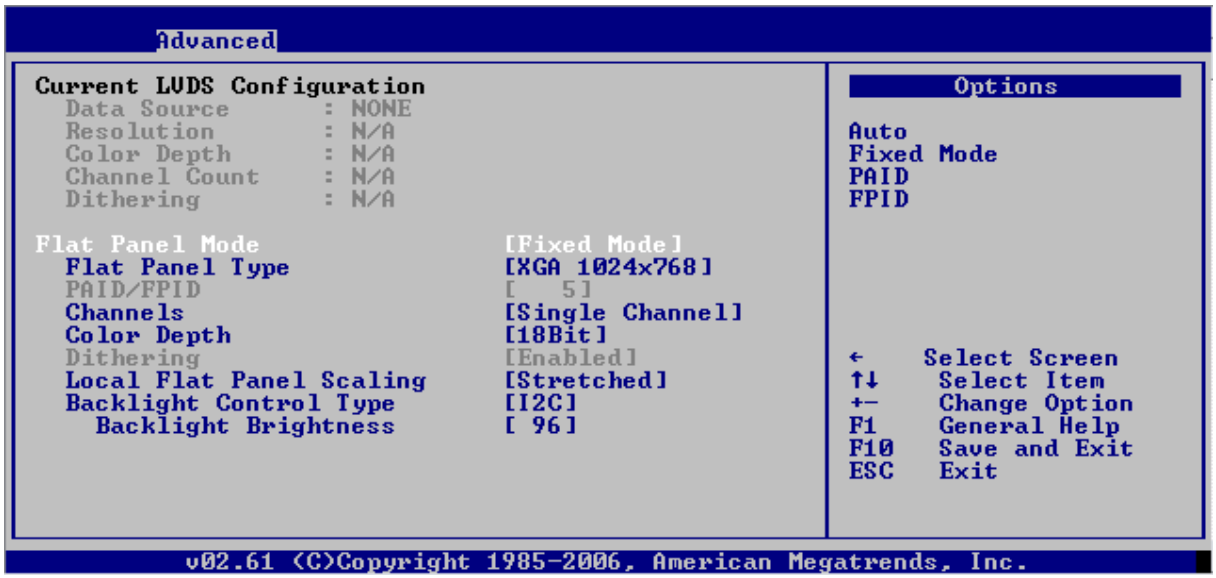
Video Function Configuration Menu



Feature	Option	Description
DVMT Mode Select	**DVMT Mode**	
DVMT/FIXED Memory	128MB **256MB** Max DVMT	Configures the amount of memory for the Dynamic Video Memory Technology
PAVP Mode	**Disabled** Light High	Configures the Protected Audio Video Path
Boot Display Device	CRT TV SDVO CRT+SDVO LVDS **CRT+LVDS**	Selects the Boot Display Devices
TV Standard	**NTSC** PAL SECAM SMPTE240M ITU-R television SMPTE295M SMPTE296M EIA-770.2 EIA-770.3	Selects the regarding TV standard for TV out interface
TV Sub-Type	**Depending on TV Standard**	Selects the regarding TV Sub-Type
HDMI DP Support	**Disabled** Enabled	Enables and disables the HDMI DP Support
HDCP Support	**Disabled** Enabled	Enables and disables the HDCP Support

Internal LVDS Configuration Menu

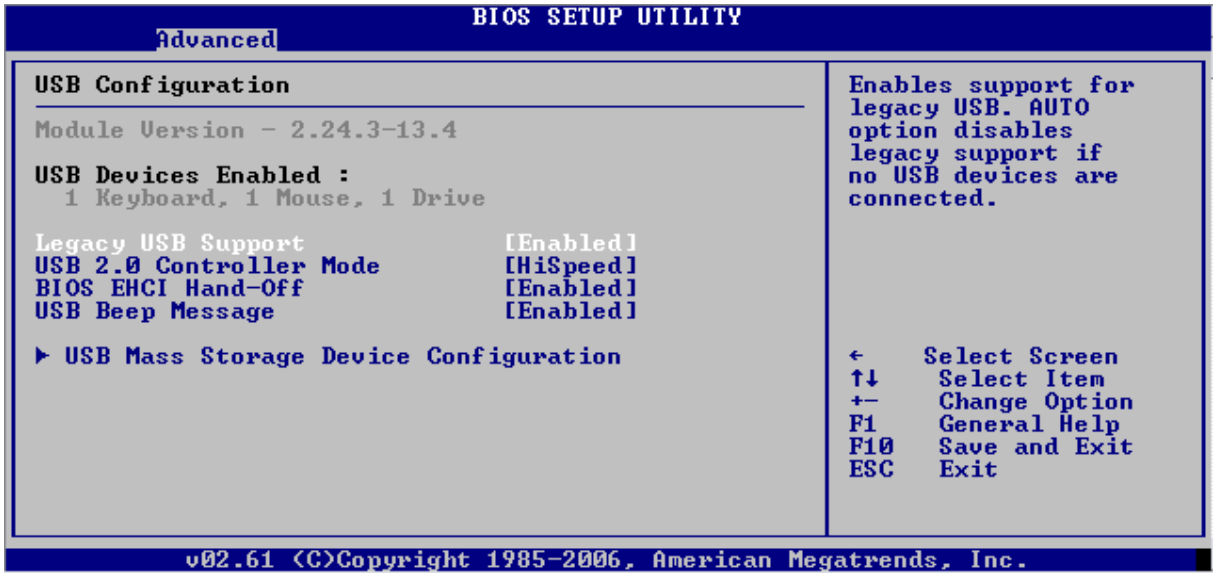




Feature	Option	Description
Flat Panel Mode	**Auto** Fixed Mode PAID FPID	Selects the Mode for the flat panel detection
Auto Fallback	**Disabled** Fixed Mode	Selects what happens, when there is no EEPROM detected (only in FPM: Auto)
Flat Panel Type	VGA 640x480 ... **XGA 1024x768** SXGA 1280x1024 ... WXGA 1280x800	Selects the resolution of the LVDS display (only in FMP: Fixed Mode)
PAID/FPID	**[X]**	Selects the number of the PAID/FPID

Channels	**Single Channel** Dual Channel	Selects, if 1x or 2x LVDS signals are used (only in FPM: Fixed Mode)
Color Depth	**18bit** 24bit open LDI 24bit	Selects the Color Depth of the connected LVDS display (only in FPM: Fixed Mode)
Local Flat Panel Scaling	Centered **Stretched** Disabled	Selects the Scaling Options for the LVDS panel (only in FPM: Fixed Mode)
LVDS -> DVI ID	[X]	5 = 1x18 7 = 2x18 8 = 1x24 A = 2x24 (only in FPM: Auto)
Backlight Control Type	None/External **I2C** PWM	Selects the mode for Backlight Control
Backlight Brightness	[0...255]	Selects the default setting for Backlight Brightness

USB Configuration Menu


BIOS SETUP UTILITY
Advanced
USB Configuration
Module Version - 2.24.3-13.4
USB Devices Enabled :
1 Keyboard, 1 Mouse, 1 Drive
Legacy USB Support [Enabled]
USB 2.0 Controller Mode [HiSpeed]
BIOS EHCI Hand-Off [Enabled]
USB Beep Message [Enabled]
▶ USB Mass Storage Device Configuration
Enables support for legacy USB. AUTO option disables legacy support if no USB devices are connected.
← Select Screen
↑↓ Select Item
+- Change Option
F1 General Help
F10 Save and Exit
ESC Exit
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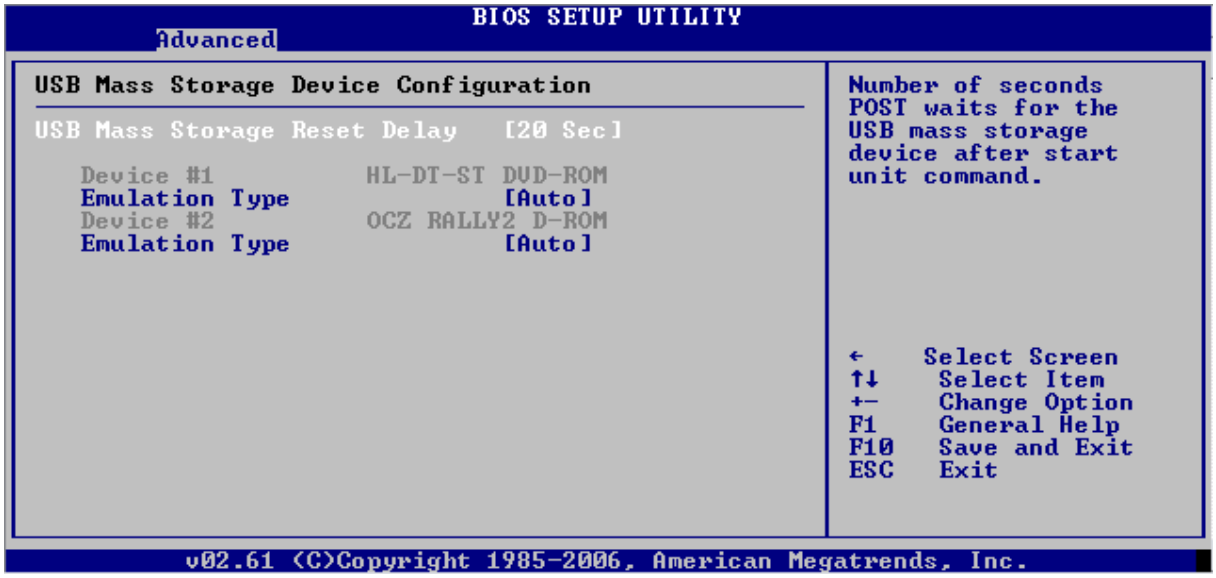
Feature	Option	Description
Legacy USB Support	Disabled **Enabled** Auto	Enables, disables or autoselects the USB legacy support feature
USB 2.0 Controller Mode	**HiSpeed** FullSpeed	Configures the USB 2.0 Controller to either HiSpeed (480Mbs) or FullSpeed (12Mbs)
BIOS EHCI Hand-Off	Disabled **Enabled**	This is a workaround for OSs without EHCI hand-off support. The EHCI ownership change should claim by EHCI driver.
USB Beep Message	Disabled **Enabled**	Enables and disables the Beep during USB device enumeration

USB Mass Storage Device Configuration Menu


BIOS SETUP UTILITY
Advanced
USB Mass Storage Device Configuration
USB Mass Storage Reset Delay [20 Sec]
Device #1 HL-DT-ST DVD-ROM
Emulation Type [Auto]
Device #2 OCZ RALLY2 D-ROM
Emulation Type [Auto]
Number of seconds POST waits for the USB mass storage device after start unit command.
← Select Screen
↑↓ Select Item
+- Change Option
F1 General Help
F10 Save and Exit
ESC Exit
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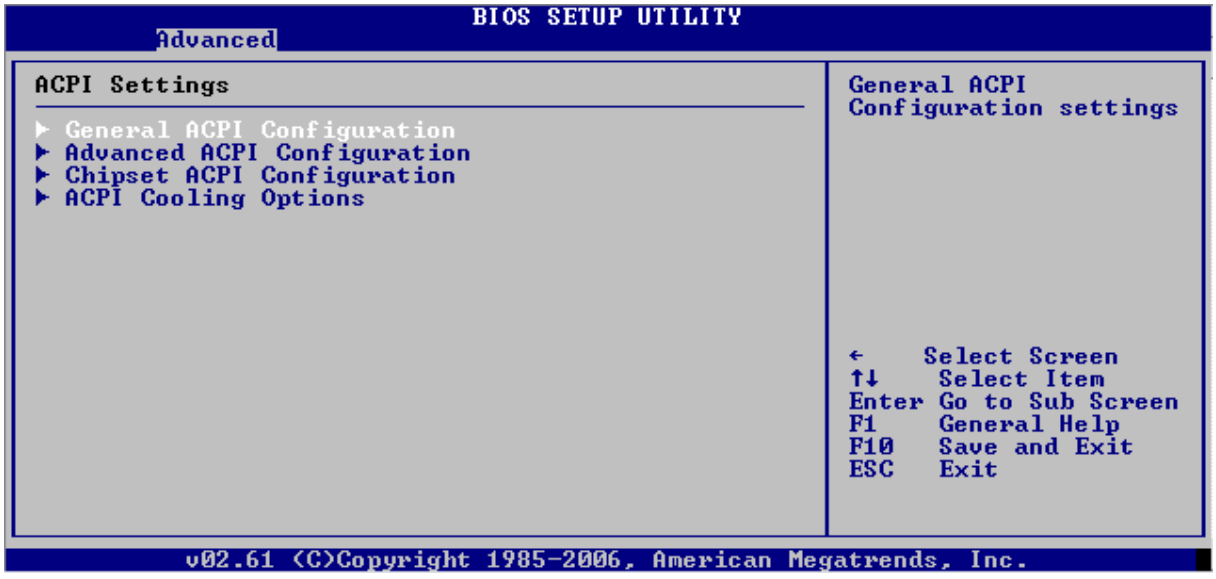
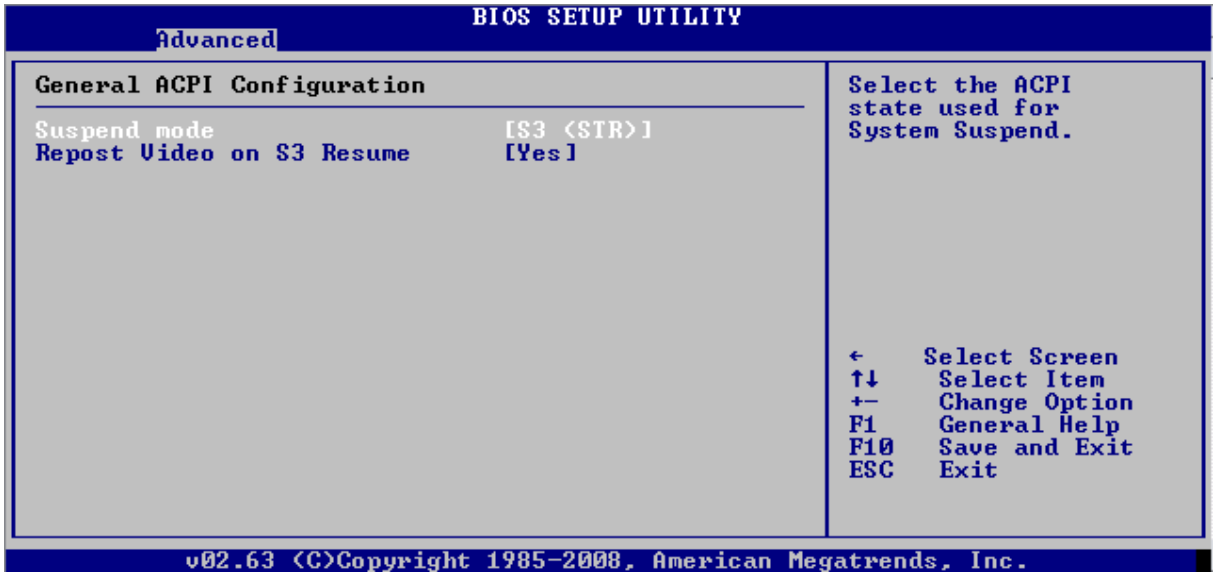
Feature	Option	Description
USB Mass Storage Reset Delay	10 Sec **20 Sec** 30 Sec 40 Sec	Number of seconds POST waits for the USB mass storage device after start unit command
Emulation Type	**Auto** Floppy Forced FDD Hard Disk CDROM	Selects the emulation type for the USB Mass Storage device

ACPI Configuration Menu

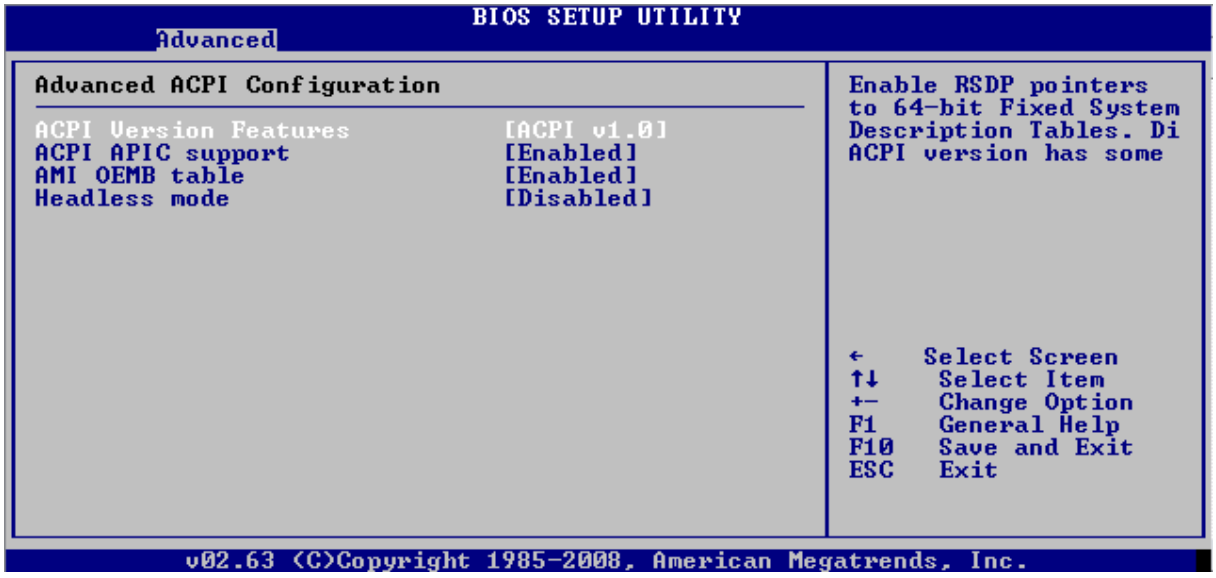


General ACPI Configuration



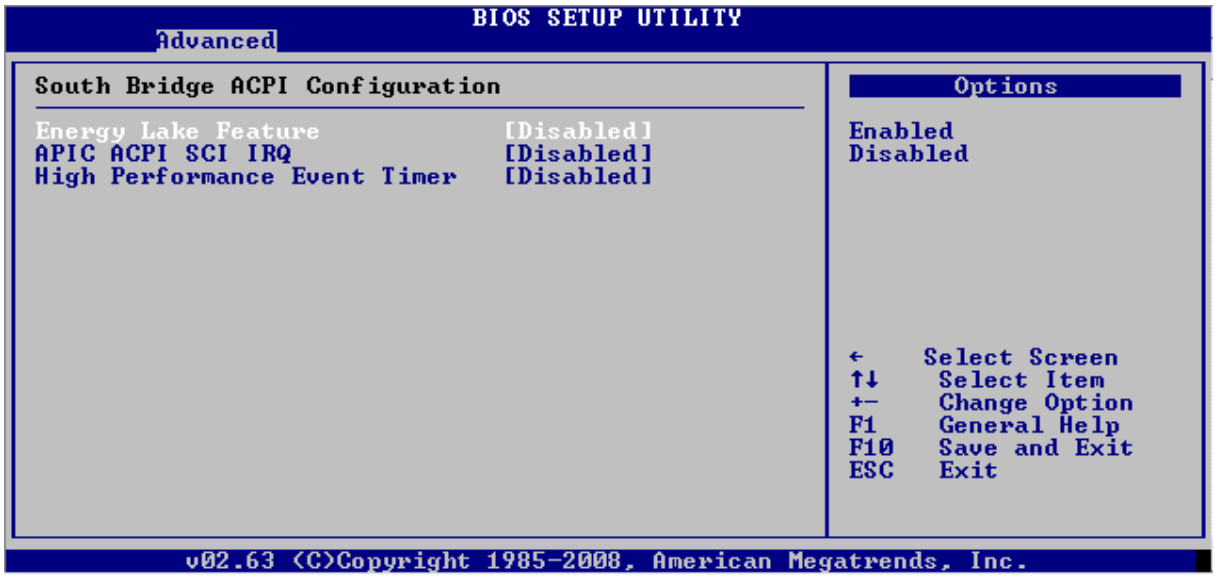
Feature	Option	Description
Suspend mode	S1 (POS) **S3 (STR)** Auto	Selects the used suspend mode
Repost Video on S3 Resume	Yes **No**	Selects, if the Video is shown directly after wake up

Advanced ACPI Configuration Menu



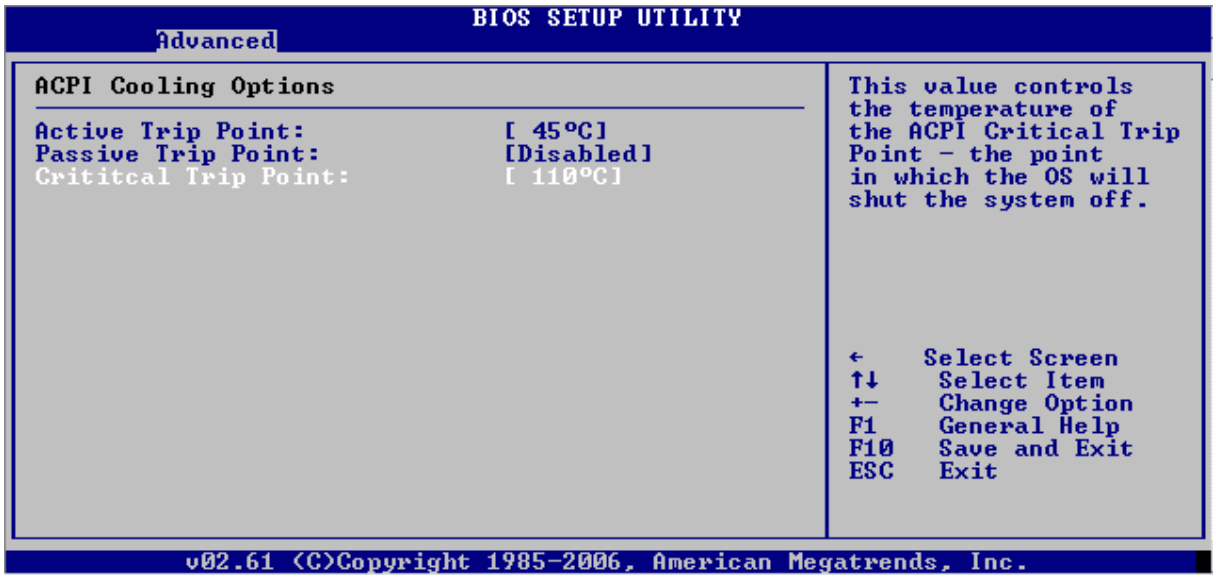
Feature	Option	Description
ACPI Version Features	ACPI v1.0 ACPI v2.0 **ACPI v3.0**	Selects the features regarding the ACPI specification version
ACPI APIC support	**Enabled** Disabled	Disables or enables the APIC support
AMI OEMB table	**Enabled** Disabled	Include OEMB table pointer to R(X)SDT pointer list
Headless mode	Enabled **Disabled**	Enable / Disable headless operation mode through ACPI

Chipset ACPI Configuration Menu



Feature	Option	Description
Energy Lake Feature	Enabled **Disabled**	Disables or enables the Energy Lake Feature of the Chipset
APIC ACPI SCI IRQ	Enabled **Disabled**	Disables or enables the APIC SCI IRQ
USB Device Wakeup from S3/S4	Enabled **Disabled**	Controls the USB device wakeup event from S3 and S4
High Performance Event Timer	Enabled **Disabled**	Disables or enables the high performance event timer
HPET Memory Address range	**FED00000h** FED01000h FED02000h FED03000h	Selects the range of the HPET memory

ACPI Cooling Options Menu


BIOS SETUP UTILITY
Advanced
ACPI Cooling Options
Active Trip Point: [45°C]
Passive Trip Point: [Disabled]
Crititcal Trip Point: [110°C]
This value controls the temperature of the ACPI Critical Trip Point - the point in which the OS will shut the system off.
← Select Screen
↑↓ Select Item
+- Change Option
F1 General Help
F10 Save and Exit
ESC Exit
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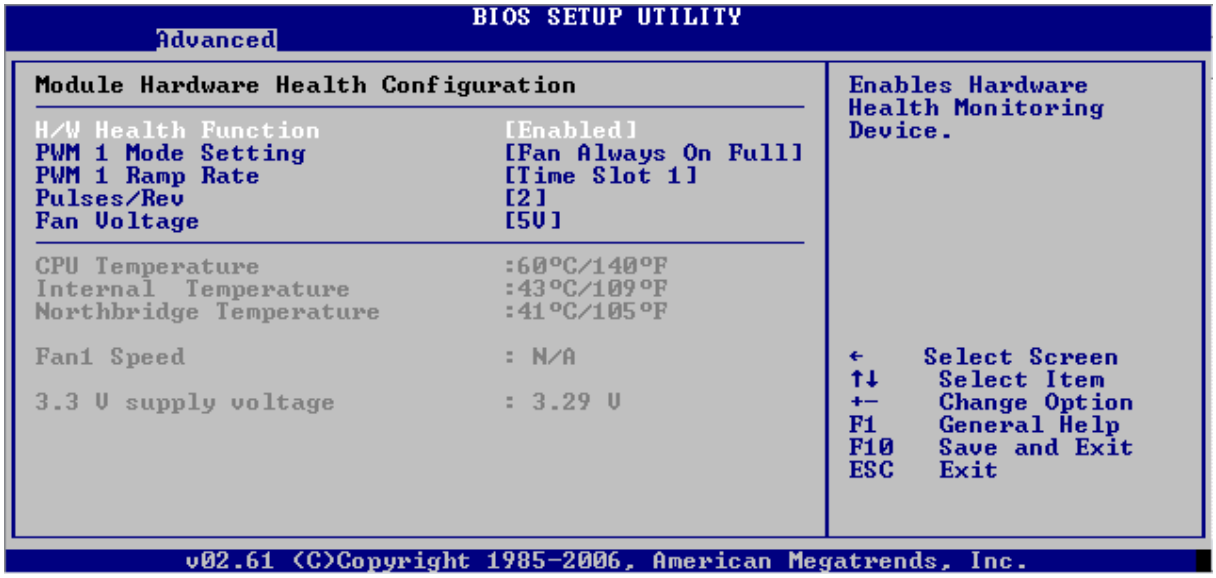
Feature	Option	Description
Active Trip Point	Disabled 40°C **45°C** 50°C 55°C ... 110°C	Set the active trip point temperature, where the fan is activated
Passive Trip Point	**Disabled** 40°C 45°C 50°C 55°C ... 110°C	Disables or enables the APIC SCI IRQ
Critical Trip Point	Disabled 40°C 45°C 50°C 55°C ... **110°C**	Disables or enables the high performance event timer

Module Hardware Health Configuration Menu

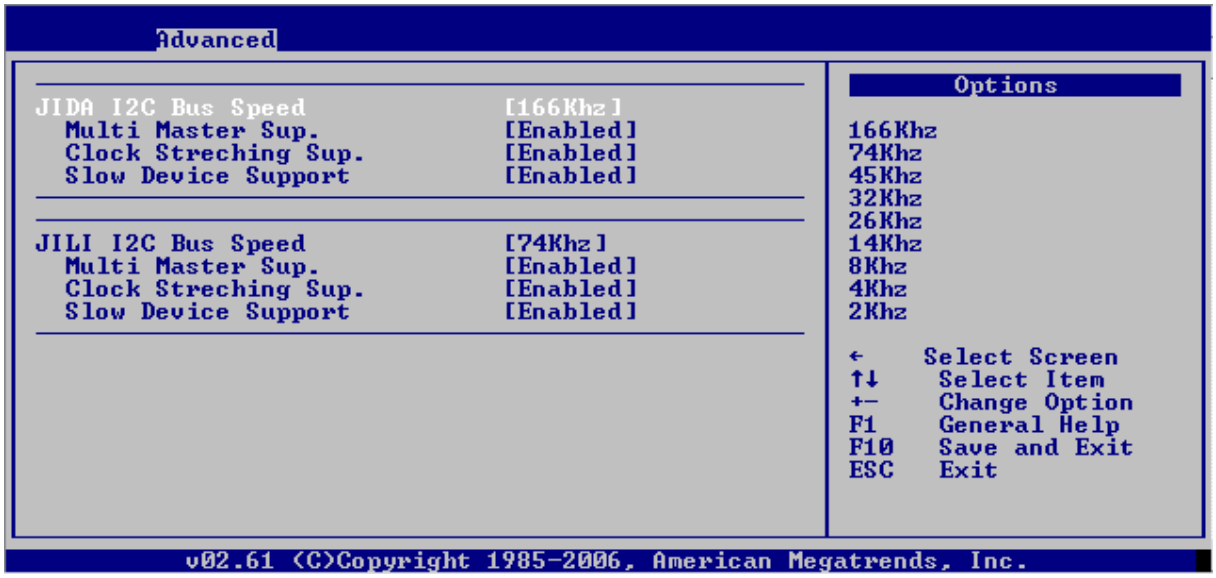


Feature	Option	Description
H/W Health Function	Disabled **Enabled**	Enables and Disables the hardware health function in BIOS setup
PWM 1 Mode Setting	Auto Fan Mode Fan Always On Full Fan Disabled Mode Fan Manually Mode	Controls the Fan interface
PWM 1 Ramp Rate	Time Slot 1 Time Slot 2 ... Time Slot 48	If enabled limits the amount of change in the PWM duty cycle over a specified period of time
Pulses / Rev	[1..4]	Selects the pulses of the fan / revision to show the correct RPMs
Fan Voltage	**5V** 12V	Selects fan voltage

Intel VT-d Configuration menu

Feature	Option	Description
Intel VT-d	**Disabled** Enabled	Enables and Disables the Intel VT-d feature

I2C Busses Menu

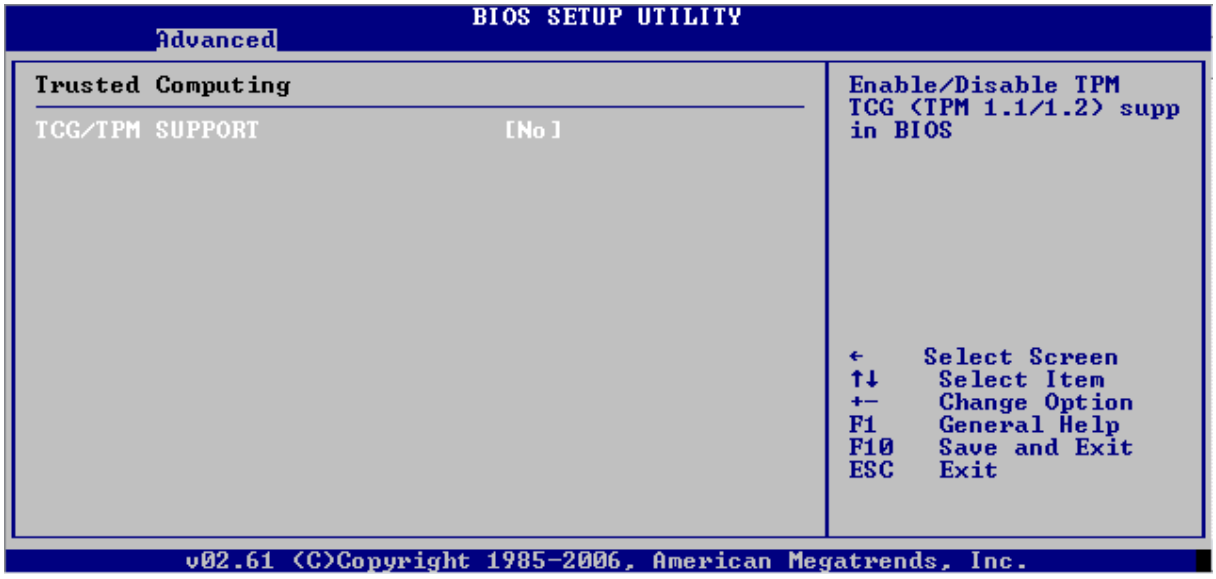


Feature	Option	Description
JIDA I2C Bus Speed	**166Khz** 74Khz 45Khz ... 2Khz	Selects the JIDA I2C Bus Speed
Multi Master Sup.	**Enabled** Disabled	Enables and disables Multi Master Support
Clock Stretching Sup.	**Enabled** Disabled	Enables and disables Clock Stretching Support
Slow Device Support	**Enabled** Disabled	Enables and disables Slow Device Support
JILI I2C Bus Speed	166Khz **74Khz** 45Khz ... 2Khz	Selects the JILI I2C Bus Speed
Multi Master Sup.	**Enabled** Disabled	Enables and disables Multi Master Support
Clock Stretching Sup.	**Enabled** Disabled	Enables and disables Clock Stretching Support
Slow Device Support	**Enabled** Disabled	Enables and disables Slow Device Support

PCIexpress Configuration Menu

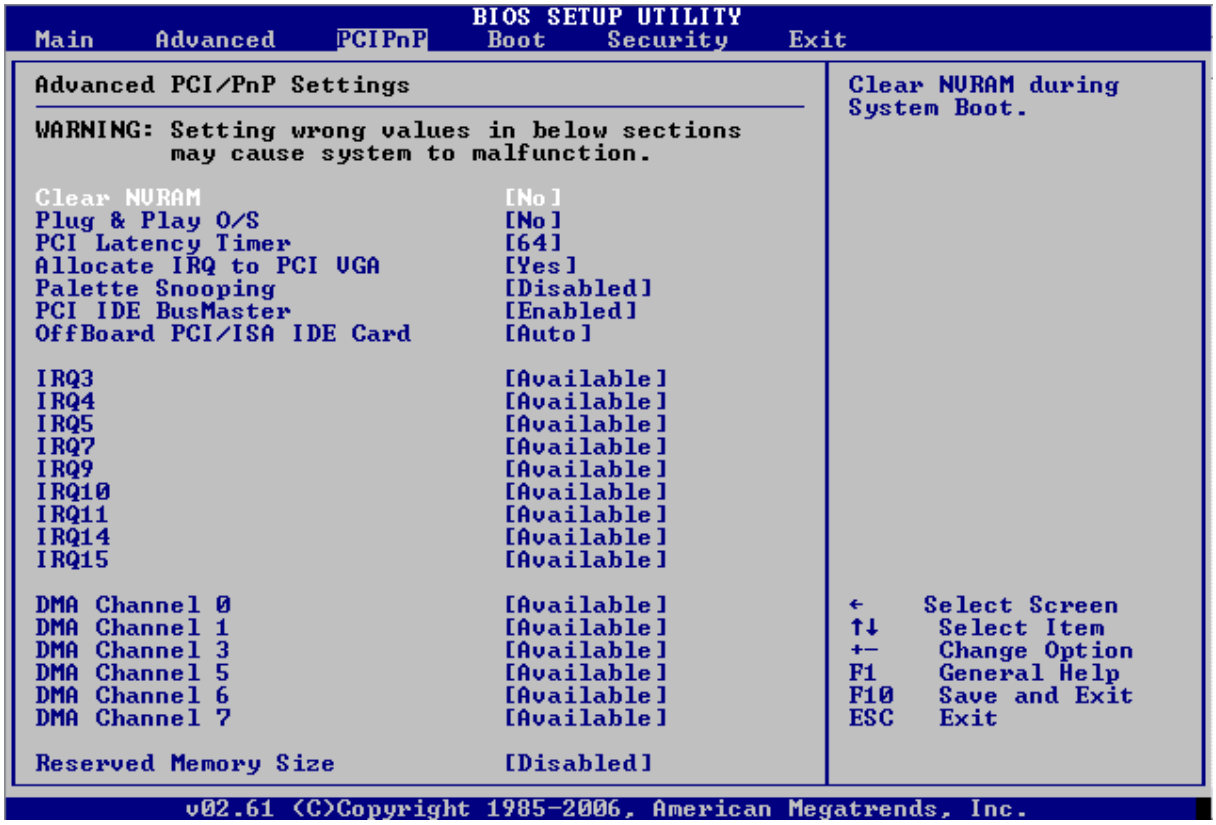
Feature	Option	Description
Active State Power-Management	**Disabled** Enabled	Enables and disables the active state power management for PCIe devices

Trusted Computing Menu



Feature	Option	Description
TCG/TPM Support	**No** Yes	Enable and disable the TCG and TPM Support

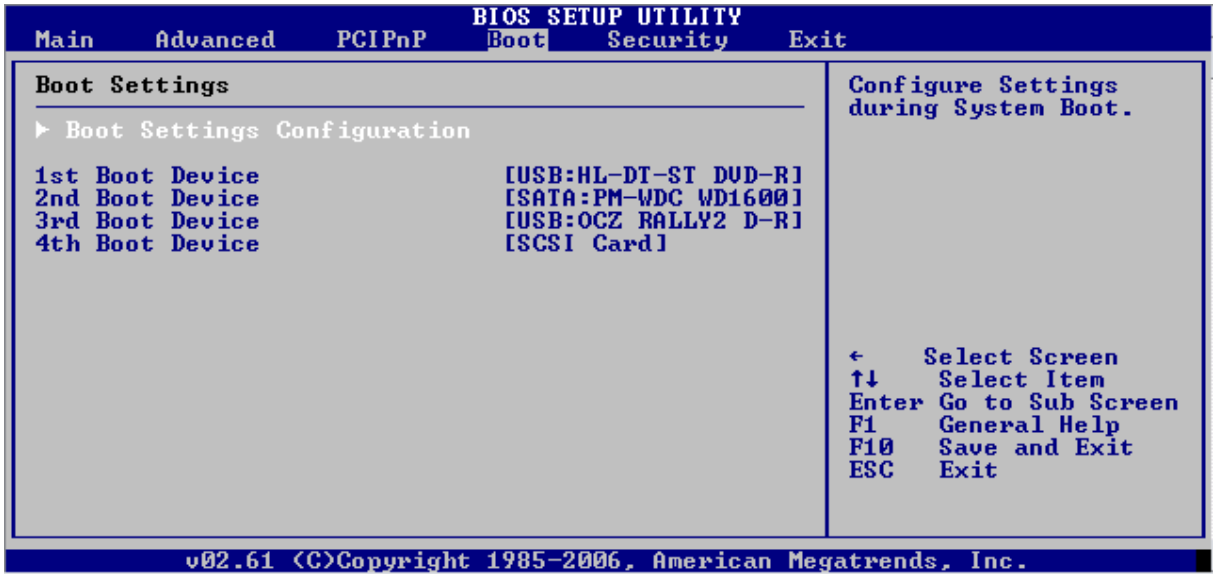
PCI/PnP Menu



Feature	Option	Description
Clear NVRAM	**No** Yes	Clear NVRAM once during next system boot.
Plug & Play O/S	**No** Yes	No: all devices are initialized by BIOS Yes: OS has to initialize some devices
PCI Latency Timer	32 **64** ... 248	Value in units of PCI clocks for PCI device latency register
Allocate IRQ to PCI VGA	**Yes** No	Decided if PCI VGA card does get an IRQ assigned if requested
Palette Snooping	**Disabled** Enabled	Disables and enables Palette Snooping
PCI IDE BusMaster	Disabled **Enabled**	Disables and enables PCI IDE Busmaster
OffBoard PCI/ISA IDE Card	**Auto** PCISlot 1 PCISlot 2 ... PCISlot 6	Some IDE Cards needs this , with set to Auto it works with most cards
IRQ3 ... IRQ15	**Available** Reserved	Available: IRQ useable by PCI/PnP devices Reserved: IRQ is reserved for ISA devices
DMA Channel 0 ... DMA Channel 7	**Available** Reserved	Available: DMA useable by PCI/PnP devices Reserved: IRQ is reserved for ISA devices
Reserved Memory Size	**Disabled** 16k 32k	Size of memory block to reserve for legacy ISA devices

	64k	

9.3.3 Boot Menu


BIOS SETUP UTILITY
Main Advanced PCIPnP Boot Security Exit
Boot Settings
Boot Settings Configuration
1st Boot Device [USB:HL-DT-ST DVD-R]
2nd Boot Device [SATA:PM-WDC WD1600]
3rd Boot Device [USB:OCZ RALLY2 D-R]
4th Boot Device [SCSI Card]
Configure Settings during System Boot.
← Select Screen
↑↓ Select Item
Enter Go to Sub Screen
F1 General Help
F10 Save and Exit
ESC Exit
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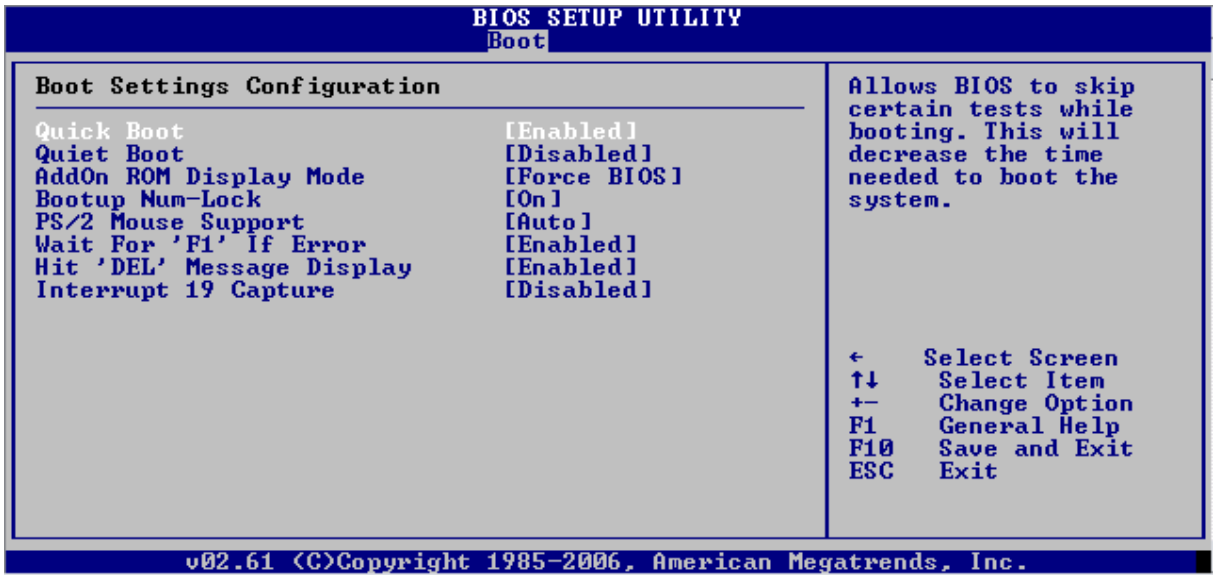
Feature	Option	Description
1st Boot Device	**Selects detected devices**	
2nd Boot Device	**Selects detected devices**	

Boot Settings Configuration


BIOS SETUP UTILITY
Boot
Boot Settings Configuration
Quick Boot [Enabled]
Quiet Boot [Disabled]
AddOn ROM Display Mode [Force BIOS]
Bootup Num-Lock [On]
PS/2 Mouse Support [Auto]
Wait For 'F1' If Error [Enabled]
Hit 'DEL' Message Display [Enabled]
Interrupt 19 Capture [Disabled]
Allows BIOS to skip certain tests while booting. This will decrease the time needed to boot the system.
← Select Screen
↑↓ Select Item
+- Change Option
F1 General Help
F10 Save and Exit
ESC Exit
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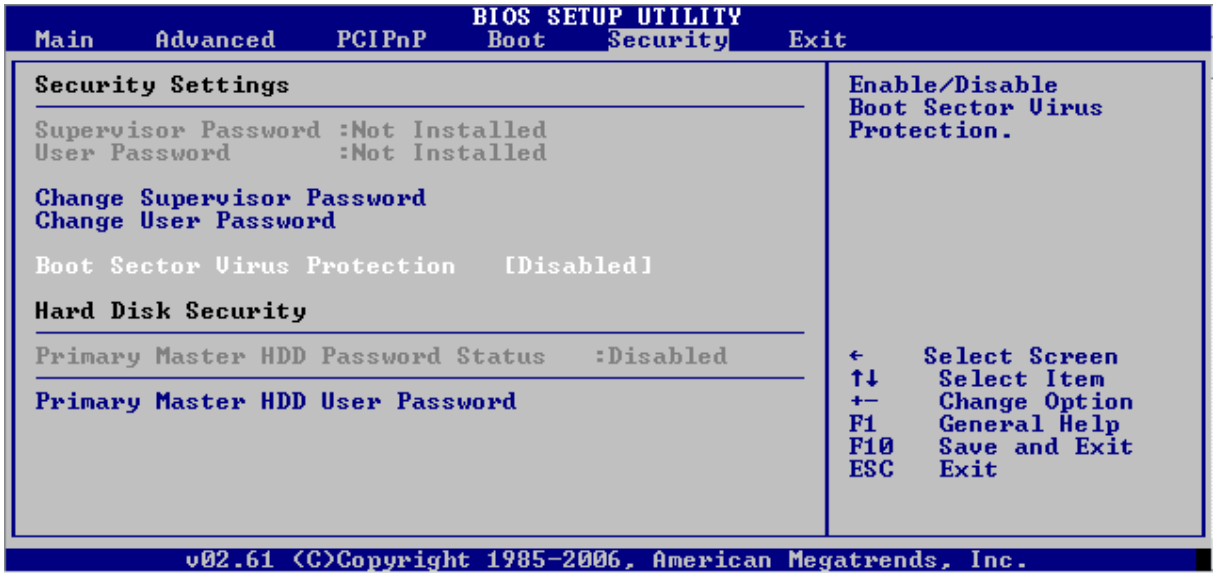
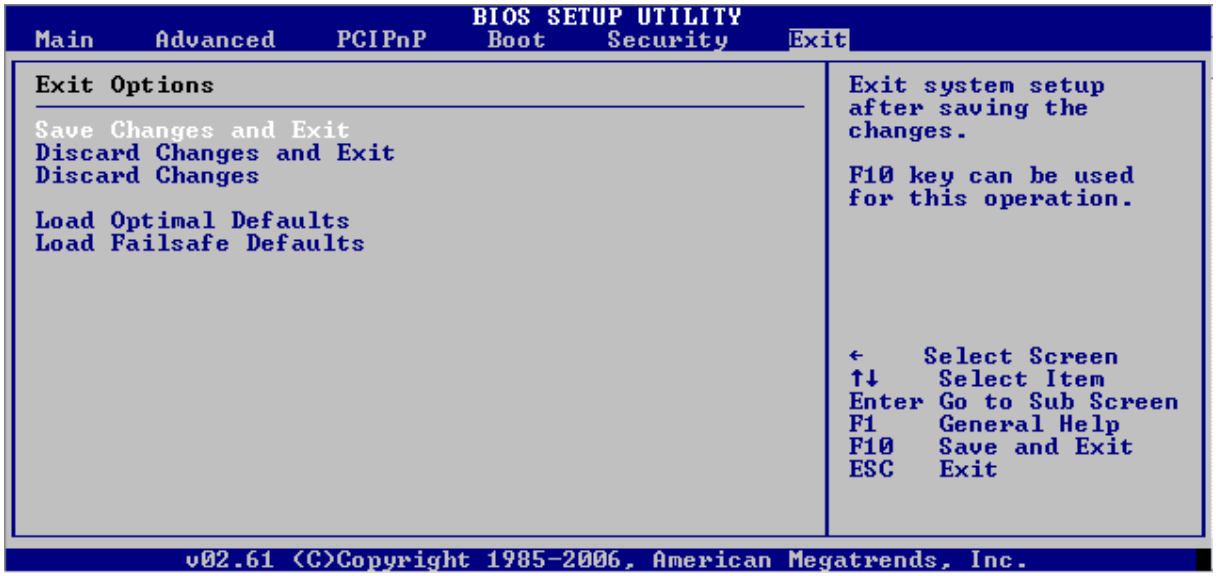
Feature	Option	Description
Quick Boot	**Enabled** Disabled	Disables or enables the quick boot feature
Quiet Boot	**Disabled** Enabled	Disabled: Shows normal POST messages Enabled: Shows OEM Logo during boot up
AddOn ROM Display Mode	**Force BIOS** Keep Current	Set Display Mode for Option ROM
Bootup Num-Lock	**On** Off	Select Power-On state for Num-Lock
PS/2 Mouse Support	**Auto** Disabled Enabled	Disables and enables or auto selects PS/2 Mouse Support
Wait For 'F1' If Error	Disabled **Enabled**	Wait for F1 key to be pressed, if error
Hit 'DEL' Message Display	**Enabled** Disabled	Displays: "Hit 'DEL' to run setup" during POST, if enabled
Interrupt 19 Capture	**Disabled** Enabled	Allows option ROMs to trap INT19h if enabled

9.3.4 Security Menu



Feature	Option	Description
Change Supervisor Password	**Type in**	
Change User Password	**Type in**	
Boot Sector Virus Protection	**Disabled** Enabled	Enables or disables boot sector virus protection.

9.3.5 Exit Menu


BIOS SETUP UTILITY
Main Advanced PCIPnP Boot Security Exit
Exit Options
Save Changes and Exit
Discard Changes and Exit
Discard Changes
Load Optimal Defaults
Load Failsafe Defaults
Exit system setup after saving the changes.
F10 key can be used for this operation.
← Select Screen
↑↓ Select Item
Enter Go to Sub Screen
F1 General Help
F10 Save and Exit
ESC Exit
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10 Appendix A: JIDA Standard

Every board with an on-board BIOS extension supports the following function calls, which supply information about the board. Jumptec Intelligent Device Architecture (JIDA) functions are called via Interrupt 15h. Functions include:

- AH=Eah
- AL=function number
- DX=4648h (security word)
- CL=board number (starting with 1)

The interrupt returns a CL≠0 if a board with the number specified in CL does not exist. CL will equal 0 if the board number exists. In this case, the content of DX determines if the operation was successful. DX=6B6Fh indicates success; other values indicate an error.

10.1 JIDA Information

To obtain information about boards that follow the JIDA standard, use the following procedure.

- Call Get BIOS ID with CL=1.
  The name of the first device installed will be returned.
  If you see the result Board exists (CL=0), increment CL, and call Get BIOS ID again.
- Repeat until you see Board not present (CL≠0).
  You now know the names of all boards within your system that follow the JIDA standard.
- You can find out more information about a specific board by calling the appropriate inquiry function with the board's number in CL.

Note: Association between board and board number may change because of configuration changes. Do not rely on any association between board and board number. Always use the procedure described above to determine the association between board and board number.

Refer to the JIDA manual in the jidai1xx.zip folder, which is available from the Kontron Embedded Modules GmbH Web site, for further information on implementing and using JIDA calls with C sample code.

11 Appendix B: Architecture Information

The following sources of information can help you better understand PC architecture.

11.1 Buses

11.1.1 ISA, Standard PS/2 – Connectors

- AT Bus Design: Eight and Sixteen-Bit ISA, E-ISA and EISA Design, Edward Solari, Annabooks, 1990, ISBN 0-929392-08-6
- AT IBM Technical Reference Vol 1&2, 1985
- ISA & EISA Theory and Operation, Edward Solari, Annabooks, 1992, ISBN 0929392159
- ISA Bus Specifications and Application Notes, Jan. 30, 1990, Intel
- ISA System Architecture, Third Edition, Tom Shanley and Don Anderson, Addison-Wesley Publishing Company, 1995, ISBN 0-201-40996-8
- Personal Computer Bus Standard P996, Draft D2.00, Jan. 18, 1990, IEEE Inc
- Technical Reference Guide, Extended Industry Standard Architecture Expansion Bus, Compaq 1989

11.1.2 PCI/104

- Embedded PC 104 Consortium
- The consortium provides information about PC/104 and PC/104-Plus technology. You can search for information about the consortium on the Web.
- PCI SIG
- The PCI-SIG provides a forum for its ~900 member companies, who develop PCI products based on the specifications that are created by the PCI-SIG. You can search for information about the SIG on the Web.
- PCI & PCI-X Hardware and Software Architecture & Design, Fifth Edition, Edward Solari and George Willse, Annabooks, 2001, ISBN 0-929392-63-9.
- PCI System Architecture, Tom Shanley and Don Anderson, Addison-Wesley, 2000, ISBN 0-201-30974-2.

11.2 General PC Architecture

- Embedded PCs, Markt&Technik GmbH, ISBN 3-8272-5314-4 (German)
- Hardware Bible, Winn L. Rosch, SAMS, 1997, 0-672-30954-8
- Interfacing to the IBM Personal Computer, Second Edition, Lewis C. Eggebrecht, SAMS, 1990, ISBN 0-672-22722-3
- The Indispensable PC Hardware Book, Hans-Peter Messmer, Addison-Wesley, 1994, ISBN 0-201-62424-9

- The PC Handbook: For Engineers, Programmers, and Other Serious PC Users, Sixth Edition, John P. Choisser and John O. Foster, Annabooks, 1997, ISBN 0-929392-36-1

11.3 Ports

11.3.1 RS-232 Serial

- EIA-232-E standard
- The EIA-232-E standard specifies the interface between (for example) a modem and a computer so that they can exchange data. The computer can then send data to the modem, which then sends the data over a telephone line. The data that the modem receives from the telephone line can then be sent to the computer. You can search for information about the standard on the Web.
- RS-232 Made Easy: Connecting Computers, Printers, Terminals, and Modems, Martin D. Seyer, Prentice Hall, 1991, ISBN 0-13-749854-3
- National Semiconductor
  The Interface Data Book includes application notes. Type “232” as search criteria to obtain a list of application notes. You can search for information about the data book on National Semiconductor’s Web site.

11.3.2 Serial ATA

- Serial AT Attachment (ATA) Working Group. This X3T10 standard defines an integrated bus interface between disk drives and host processors. It provides a common point of attachment for systems manufacturers and the system. You can search for information about the working group on the Web. We recommend you also search the Web for information on 4.2 I/O cable, if you use hard disks in a DMA3 or PIO4 mode.

11.3.3 USB

- USB Specification.
- USB Implementers Forum, Inc. is a non-profit corporation founded by the group of companies that developed the Universal Serial Bus specification. The USB-IF was formed to provide a support organization and forum for the advancement and adoption of Universal Serial Bus technology. You can search for information about the standard on the Web.

11.4 Programming

- C Programmer’s Guide to Serial Communications, Second Edition, Joe Campbell, SAMS, 1987, ISBN 0-672-22584-0
- Programmer’s Guide to the EGA, VGA, and Super VGA Cards, Third Edition, Richard Ferraro, Addison-Wesley, 1990, ISBN 0-201-57025-4

- The Programmer's PC Sourcebook, Second Edition, Thom Hogan, Microsoft Press, 1991, ISBN 1-55615-321-X
- Undocumented PC, A Programmer's Guide to I/O, CPUs, and Fixed Memory Areas, Frank van Gilluwe, Second Edition, Addison-Wesley, 1997, ISBN 0-201-47950-8

12 Appendix C: Document Revision History

Revision	Date	Edited by	Changes
0.1_pre	20.08.08	UMA	Created preliminary manual.
0.2_pre	25.11.08	UMA	Added supply current tables
0.3_pre	26.11.08	UMA	Exchanged product picture, added onboard fan connector description, and description for HDMI and Displayport
0.4_pre	1.12.08	UMA	Added chapter 5.3 usage of different graphic interfaces
0.5_pre	21.04.09	UMA	Added BIOS Setup description
1.0	08.05.09	UMA	Added Resource List